ESD Electronic Systems Design

Synthesis Verification Testing Power Communication

Network simulation with SystemC

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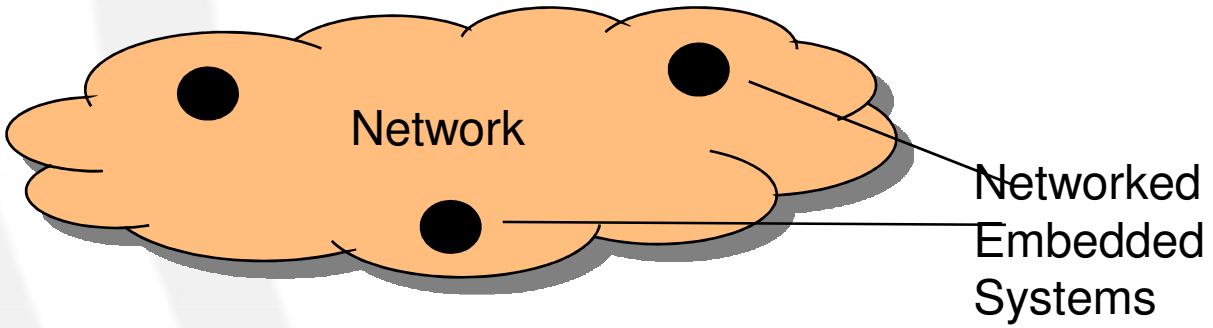
Outline

- Motivation
- Architecture
- Experimental results
- Advantages of the proposed framework

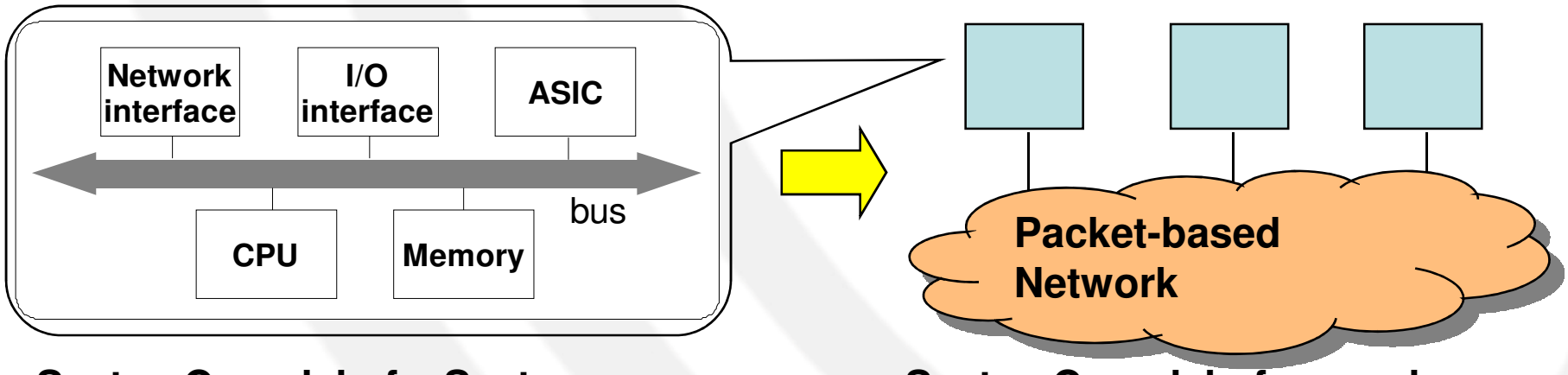
Motivation



- Design of Networked Embedded Systems (smartphones, routers, wireless sensor networks)
- Network (protocols and channels) may be a design-space dimension (e.g., Networked Control Systems)
- System and Network may be reciprocally affected during design
- Pure network simulators are not well integrated with EDA tools

SystemC Network Simulation Library (SCNSL)

Let's change the scale !



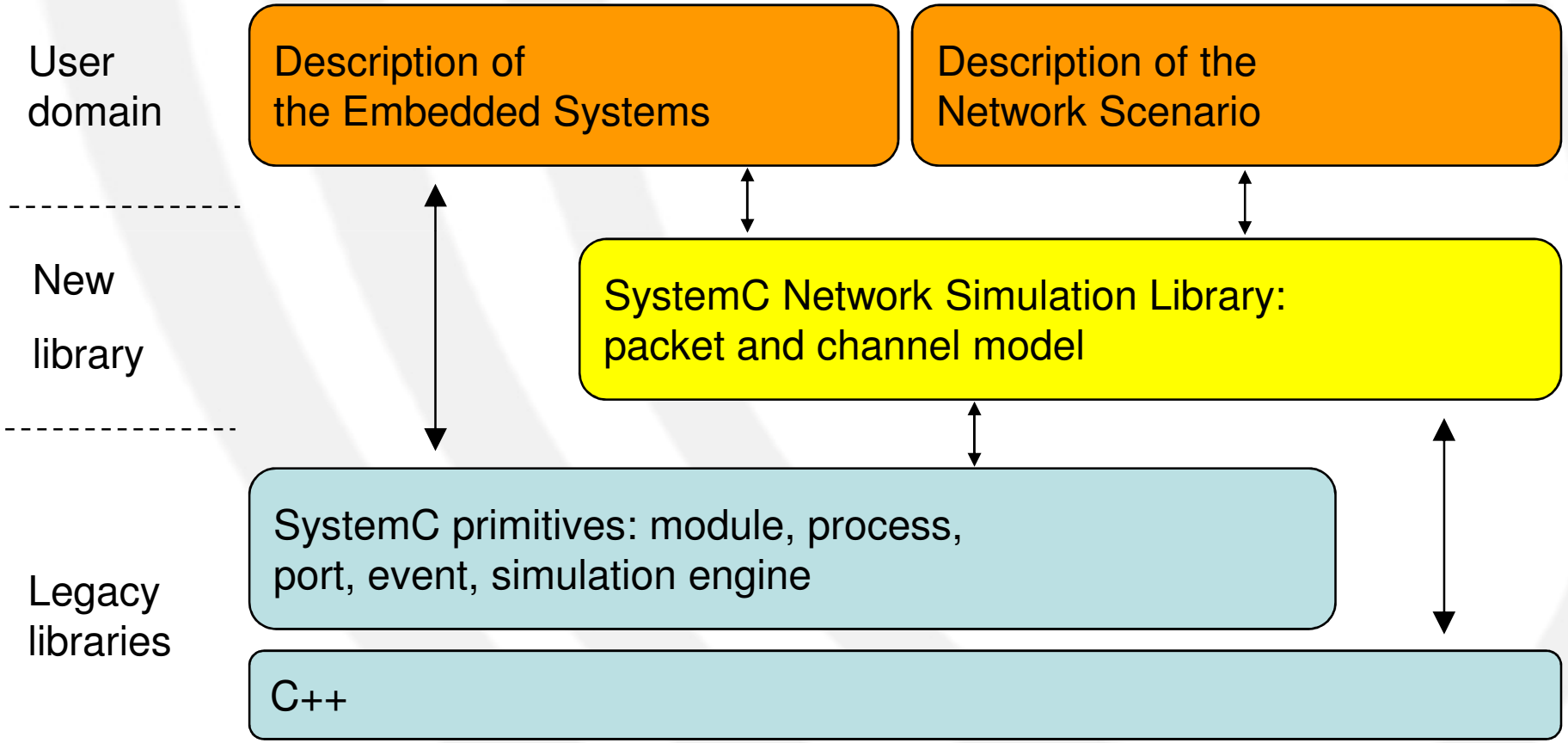
SystemC model of a System on Chip

SystemC model of several networked embedded systems AND the network among them

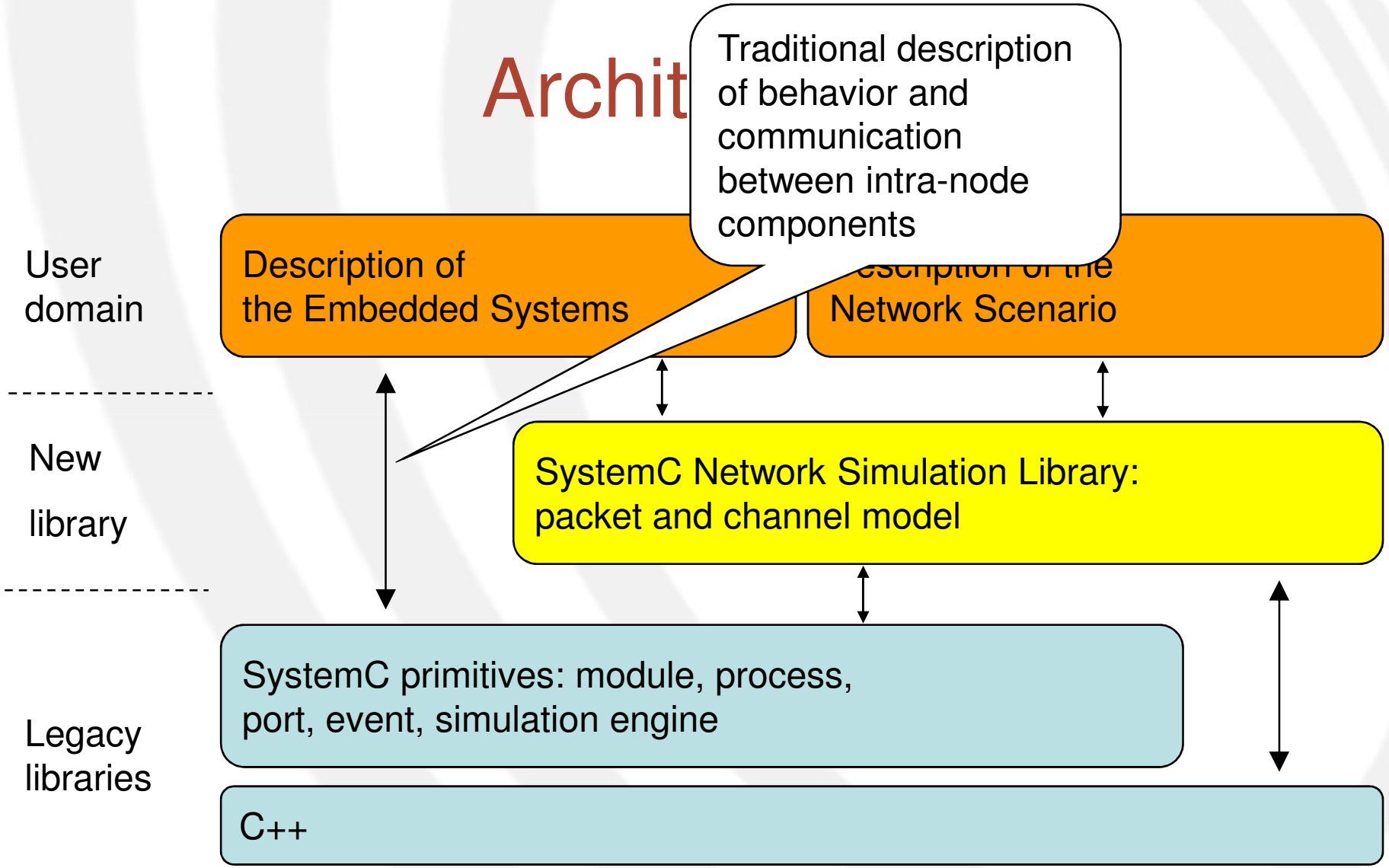
Problems to be solved

- Packet-based simulation in order to be fast
- Packets are not Signals (RTL) or Payloads (TLM)
  - Variable size
  - Variable formats (during simulation !)
- Network simulation requires that setup can change at simulation time (binding is not enough)
  - Traffic activation/de-activation
  - Node mobility
  - Channel failure
- Efficient way to handle collisions on the channel

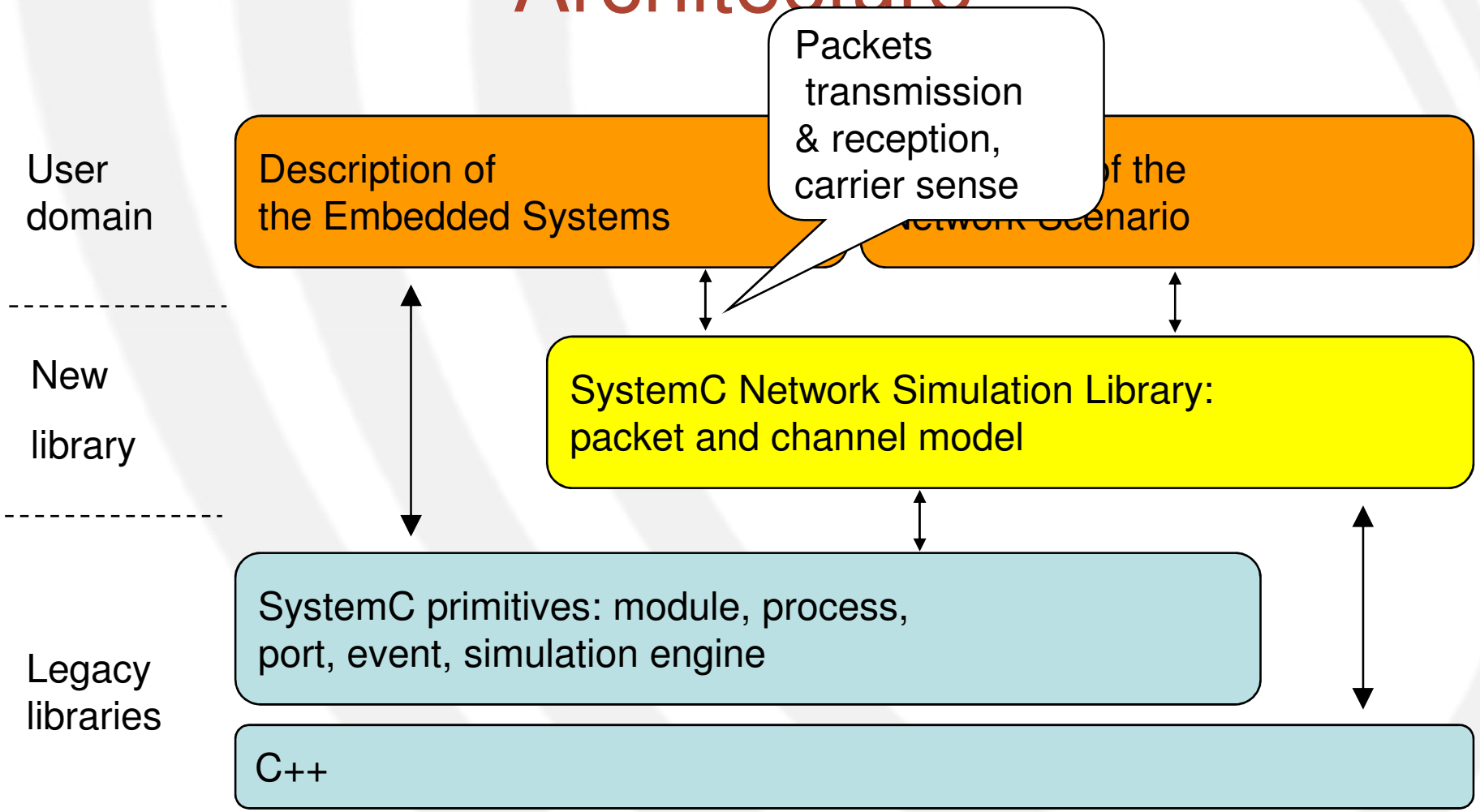
Architecture



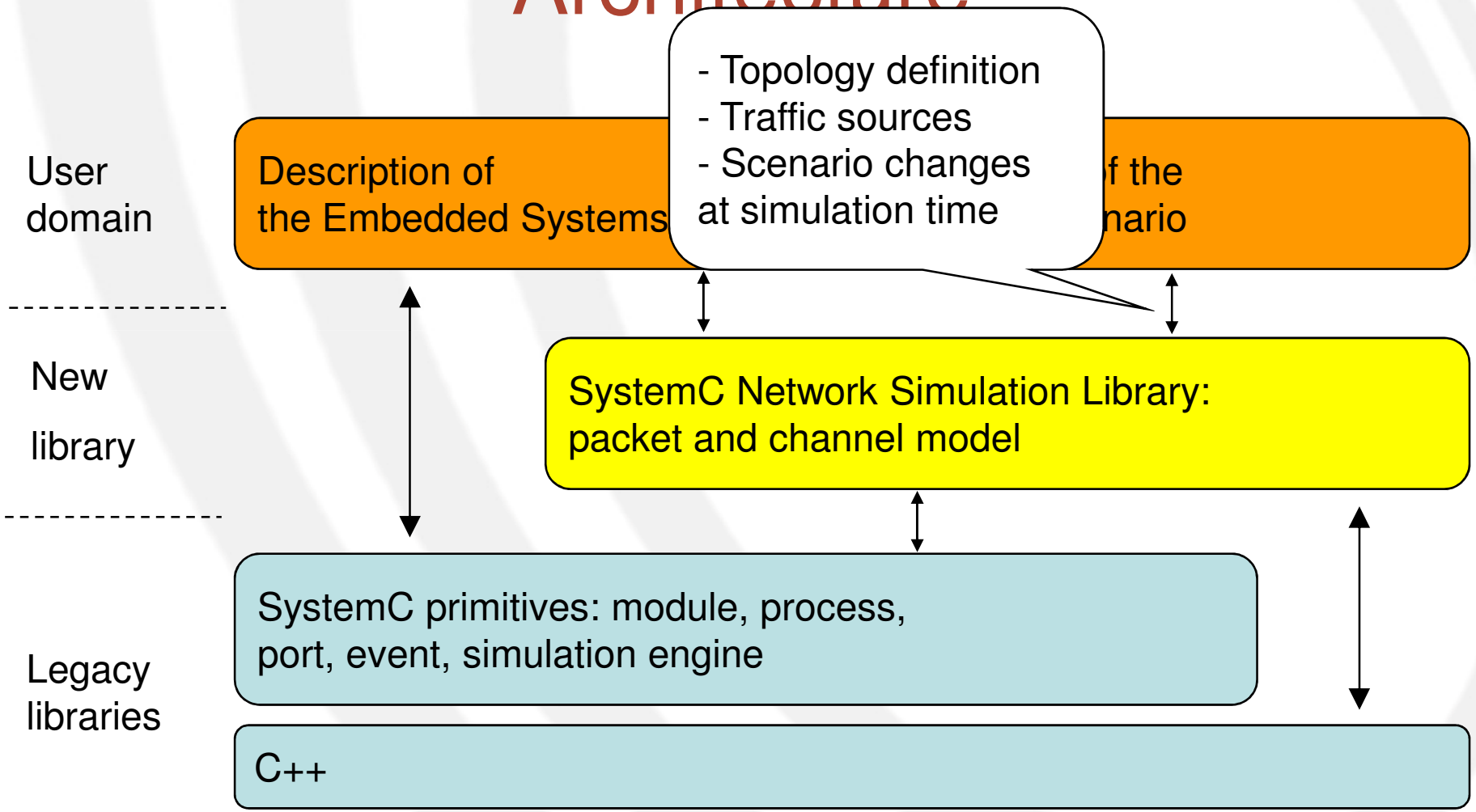
Archit


Traditional description of behavior and communication between intra-node components
User domain
Description of the Embedded Systems
Network Scenario
New library
SystemC Network Simulation Library: packet and channel model
Legacy libraries
SystemC primitives: module, process, port, event, simulation engine
C++

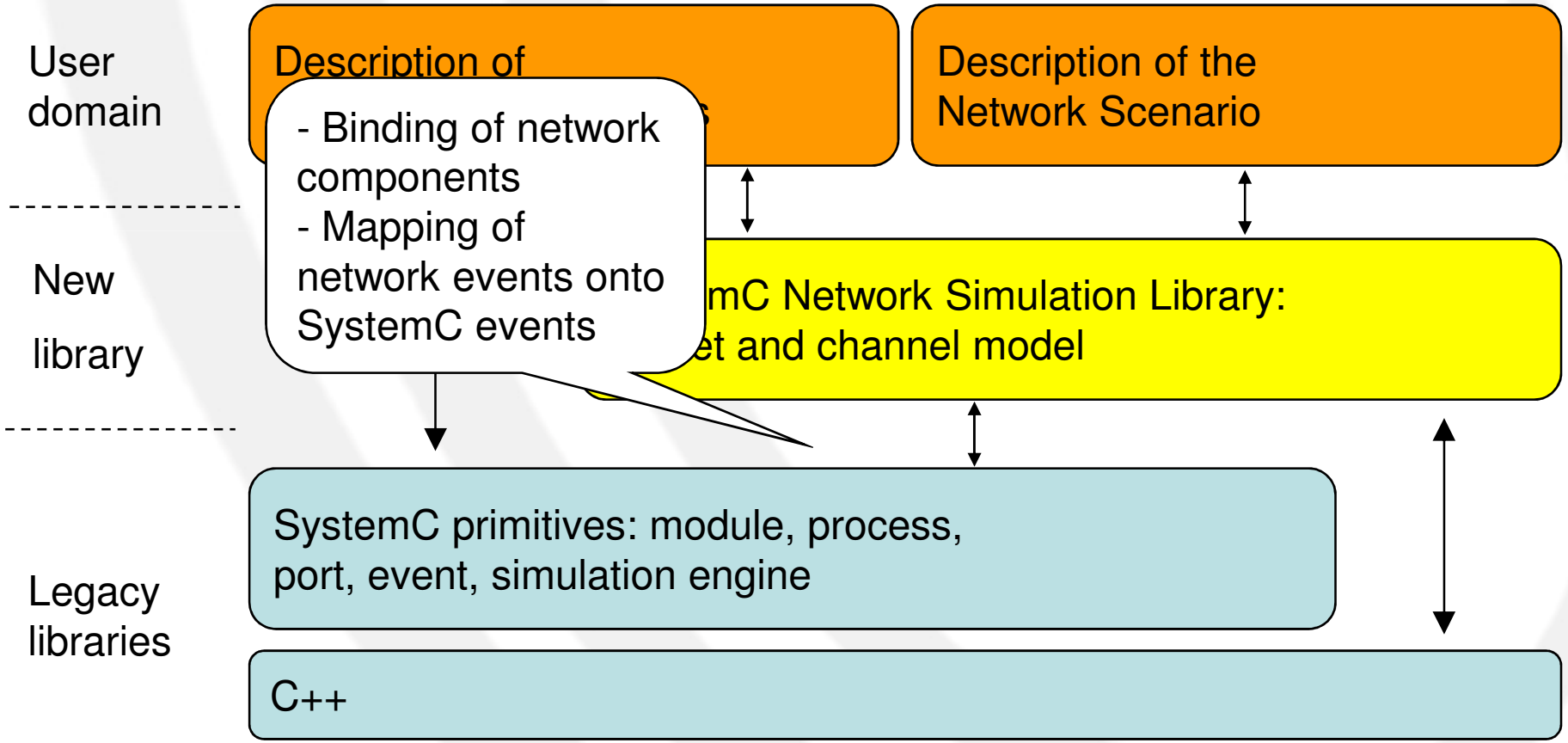
Architecture



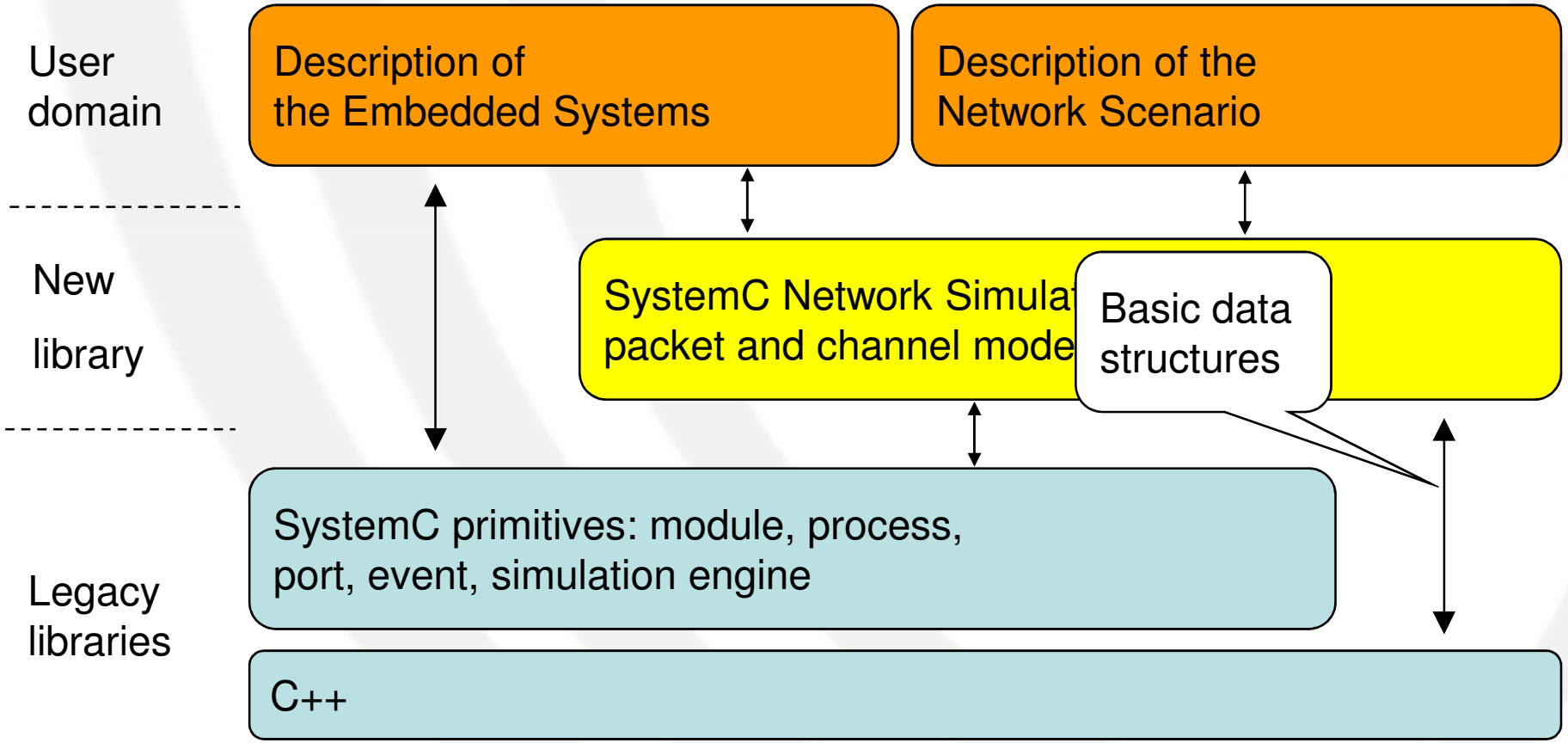
Architecture



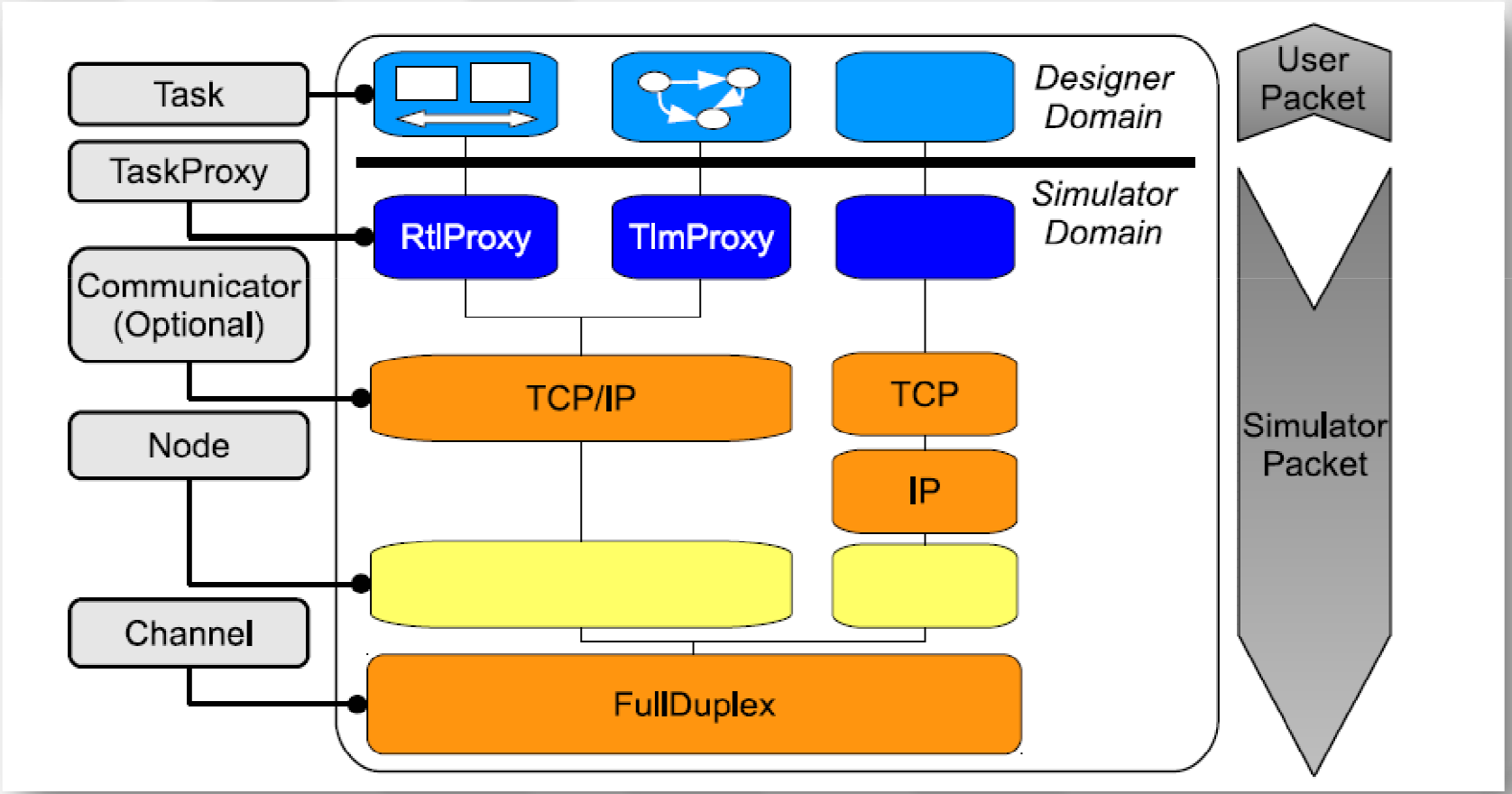
Architecture



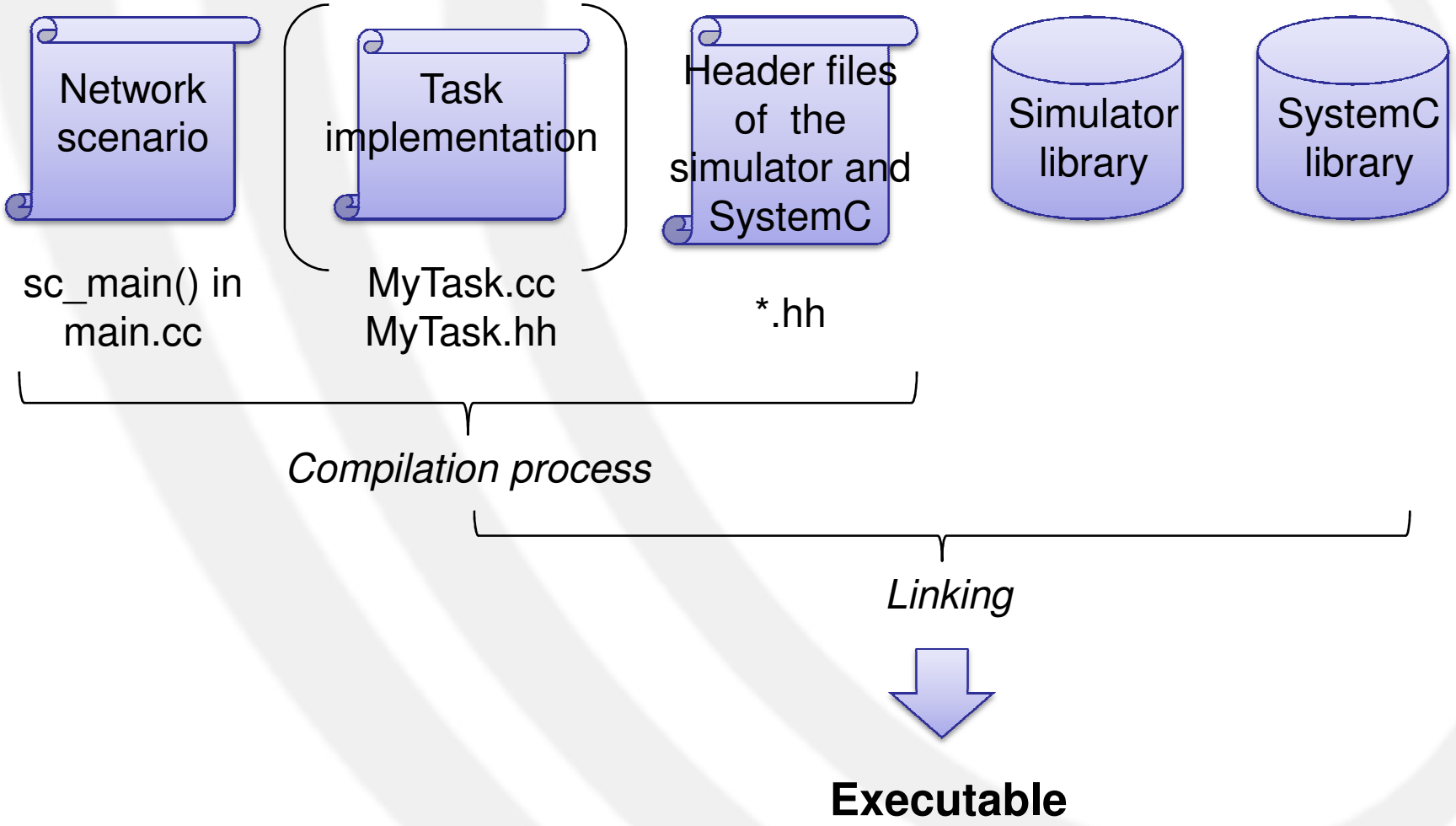
Architecture



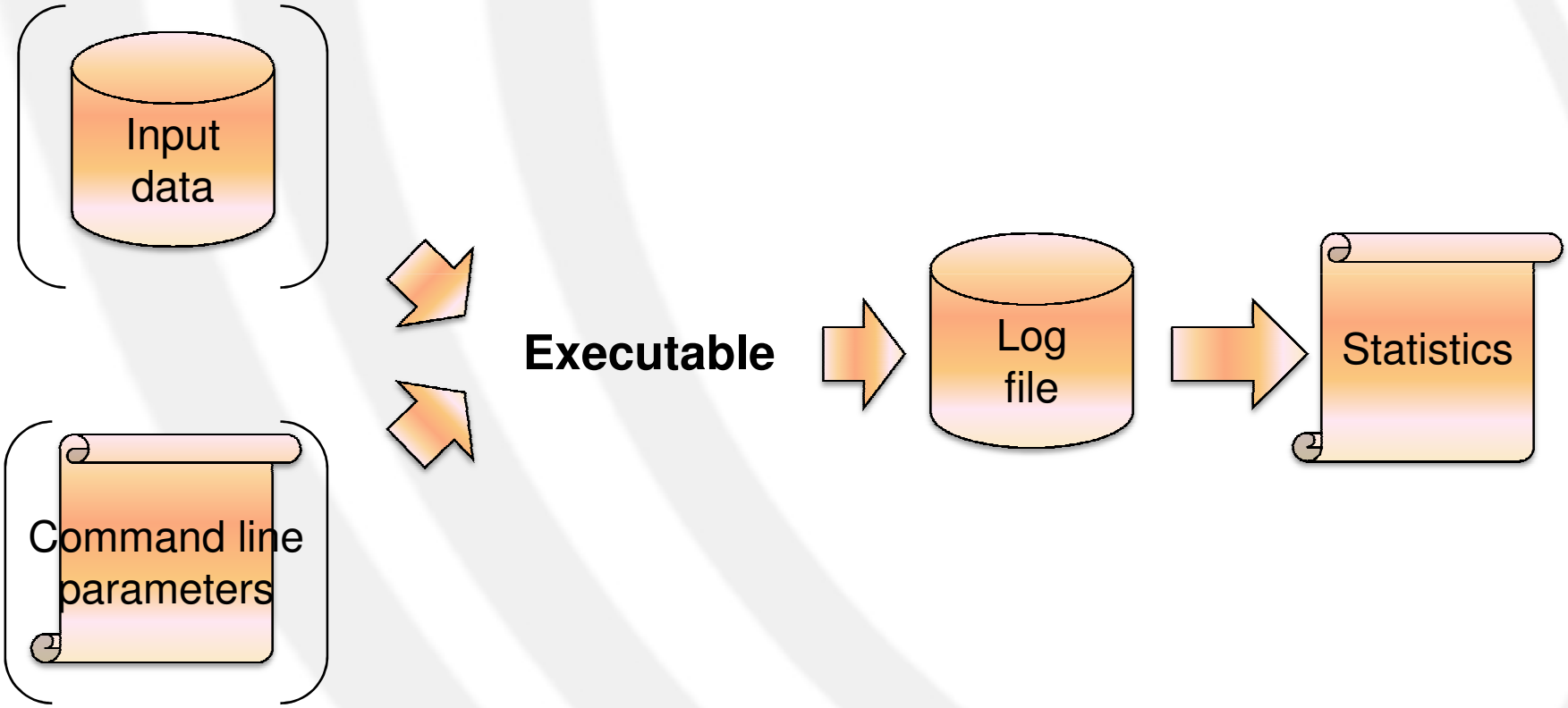
SCNSL components



Simulation flow



Simulation flow (2)



Provided objects

- Task
  - Interfaces for TLM and RTL custom tasks
  - Traffic sources (CBR, bursty traffic, etc.)
- Node
- Protocol
- Channel
  - Simple link
  - Full duplex link
  - Shared
  - Delayed shared

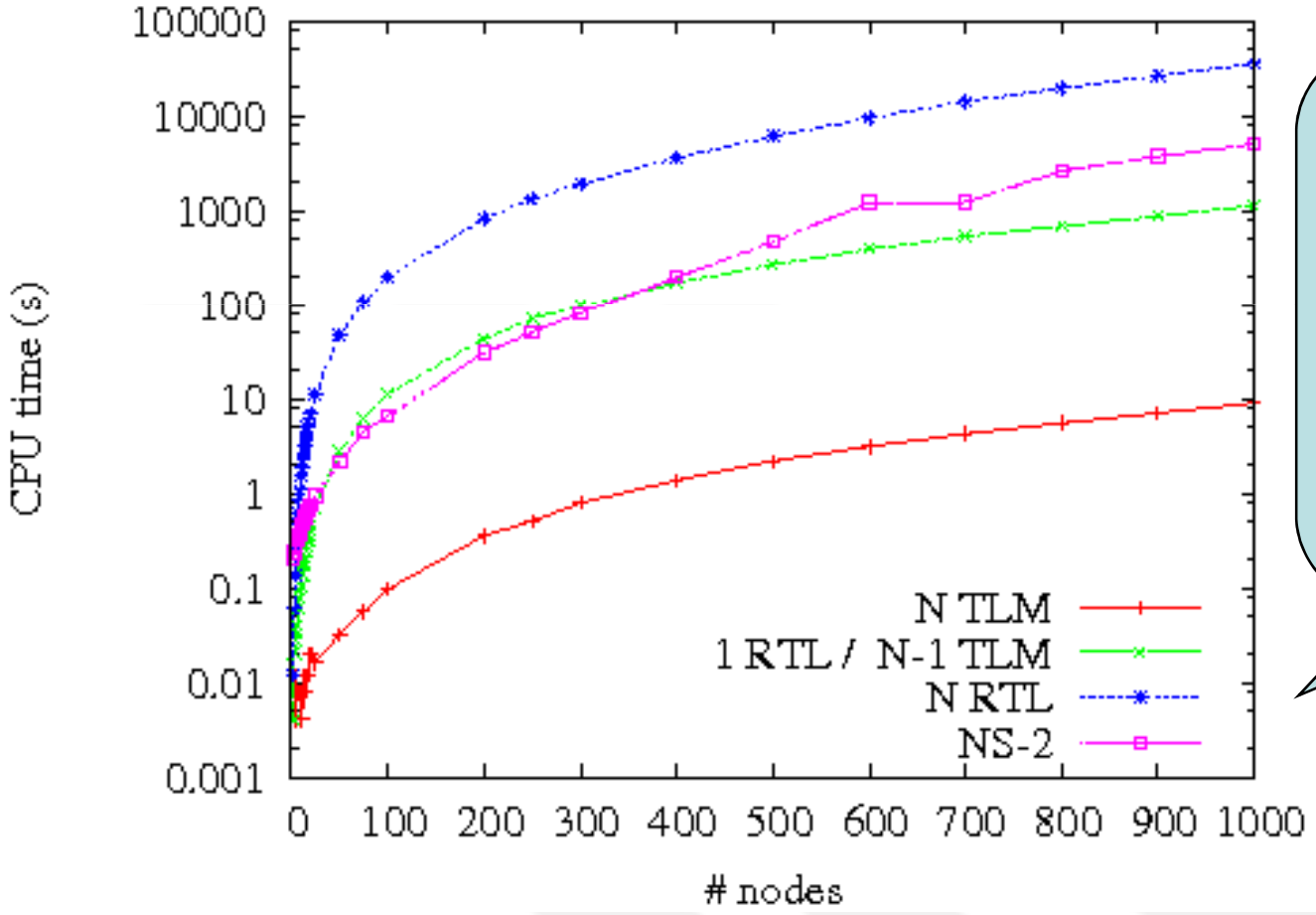
To model wired or abstract channels

To model wireless channels

Experimental setup

- Wireless sensor network
  - 1 master requesting temperature to N-1 slaves
  - IEEE 802.15.4 MAC (the base for ZigBee)
  - Peer un-slotted communication with ack
- Description of the node at different abstraction levels
  - TLM (Approximate Timing) → 633 lines of code
  - RTL → 688 lines
  - `sc_main()` → 172 lines
- Comparison with a well-known network simulator (NS-2)

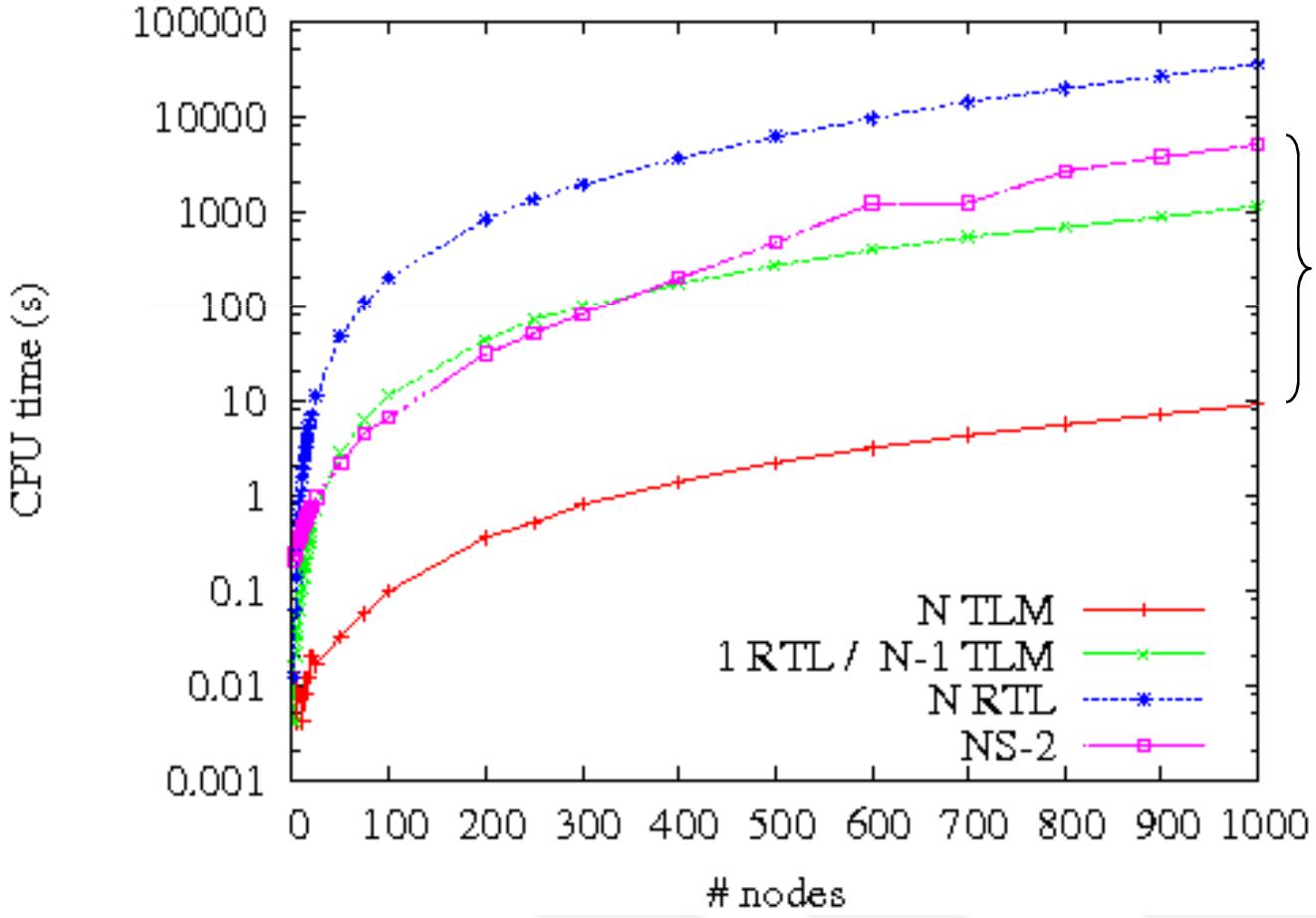
Experimental results



CPU time for the simulation as a function of the number of wireless sensor nodes.

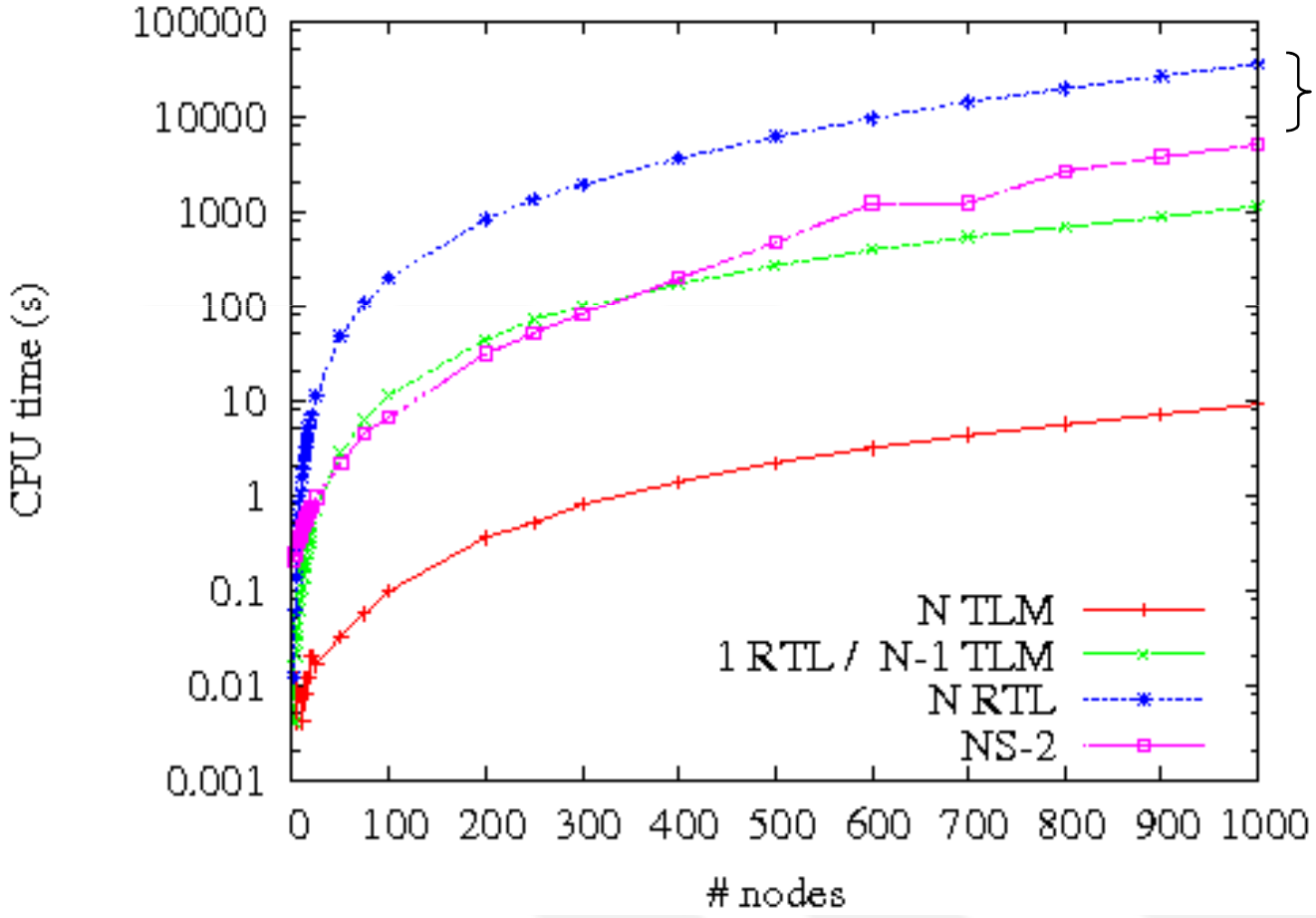
Uniix “time” command (system+user)

Experimental results



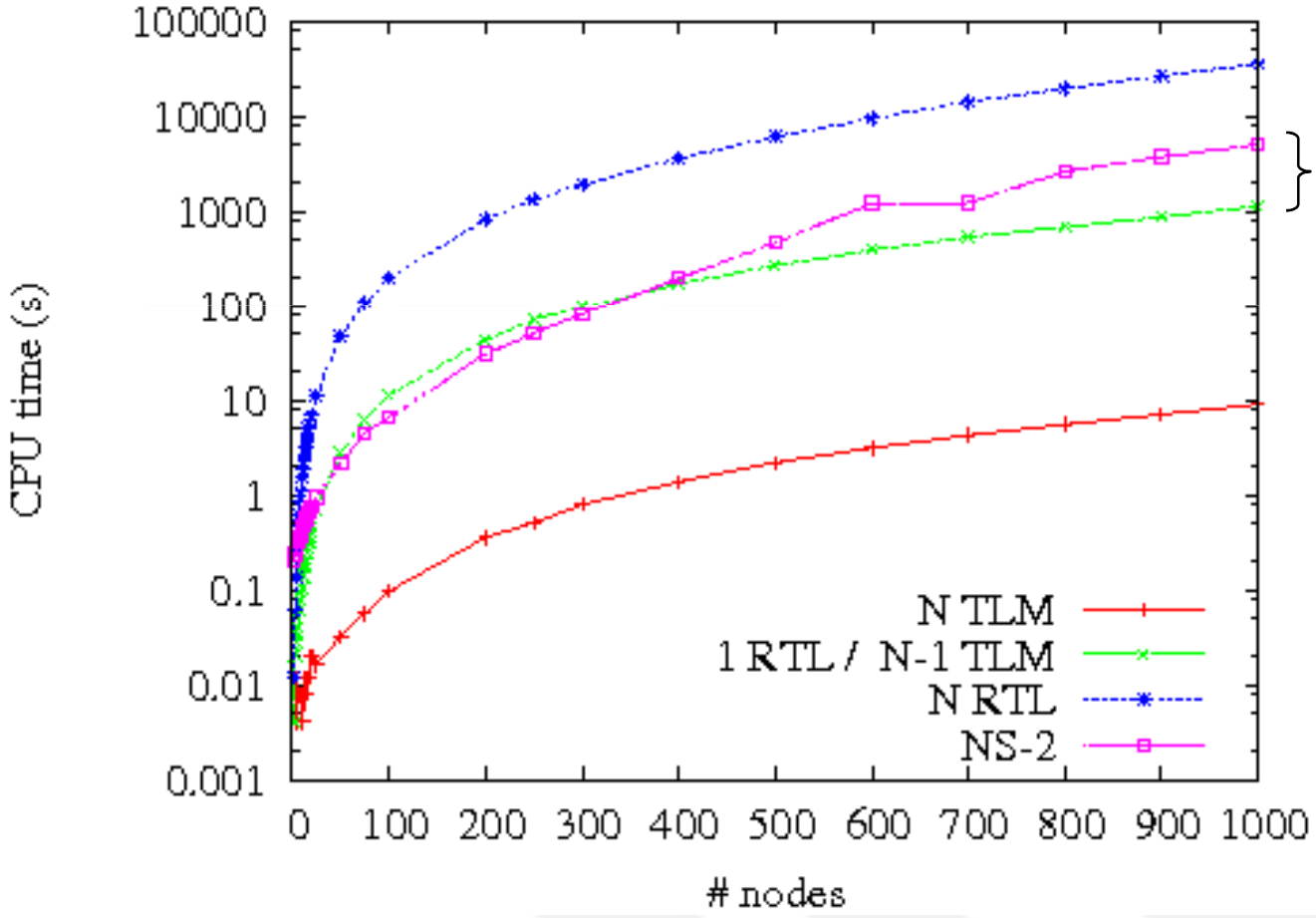
Simulation of all nodes at TLM is x100 faster than NS-2

Experimental results



Simulation of all nodes at RTL is slower than NS-2 as expected

Experimental results



Simulation of one node at RTL and the others at TLM is as fast as NS-2 with the advantage of a higher system accuracy

Fine-tuning between speed and accuracy

Advantages

- Direct use of SystemC models in network simulation → **re-usability**
- Single simulation tool (no need of System/Network co-simulation) → **fast**
- Direct support of tools from EDA ecosystem
  - SystemC TLM 2.0
  - SystemC Verification Library
  - SystemC Analog & Mixed Signals (AMS)
  - Debugging tools
  - Analysis tools
  - Synthesis

Advantages (cont.)

- Fruitful integration of Network design & simulation in the traditional design flow
- Open-source (LGPL) project on SourceForge
  - Repository with versioning
  - Bug tracking facility
  - Wiki
  - Mailing lists