Design flow for Networked Embedded Systems

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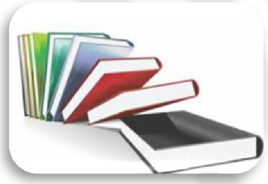
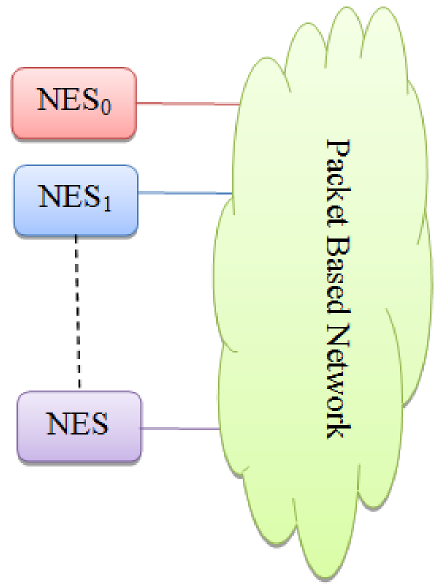
Outline



- Introduction and motivation
- Background
- Proposed methodology
- Modeling requirements
- System view simulation
- Network synthesis
- Network view simulation
- Case study
- Conclusion

Introduction

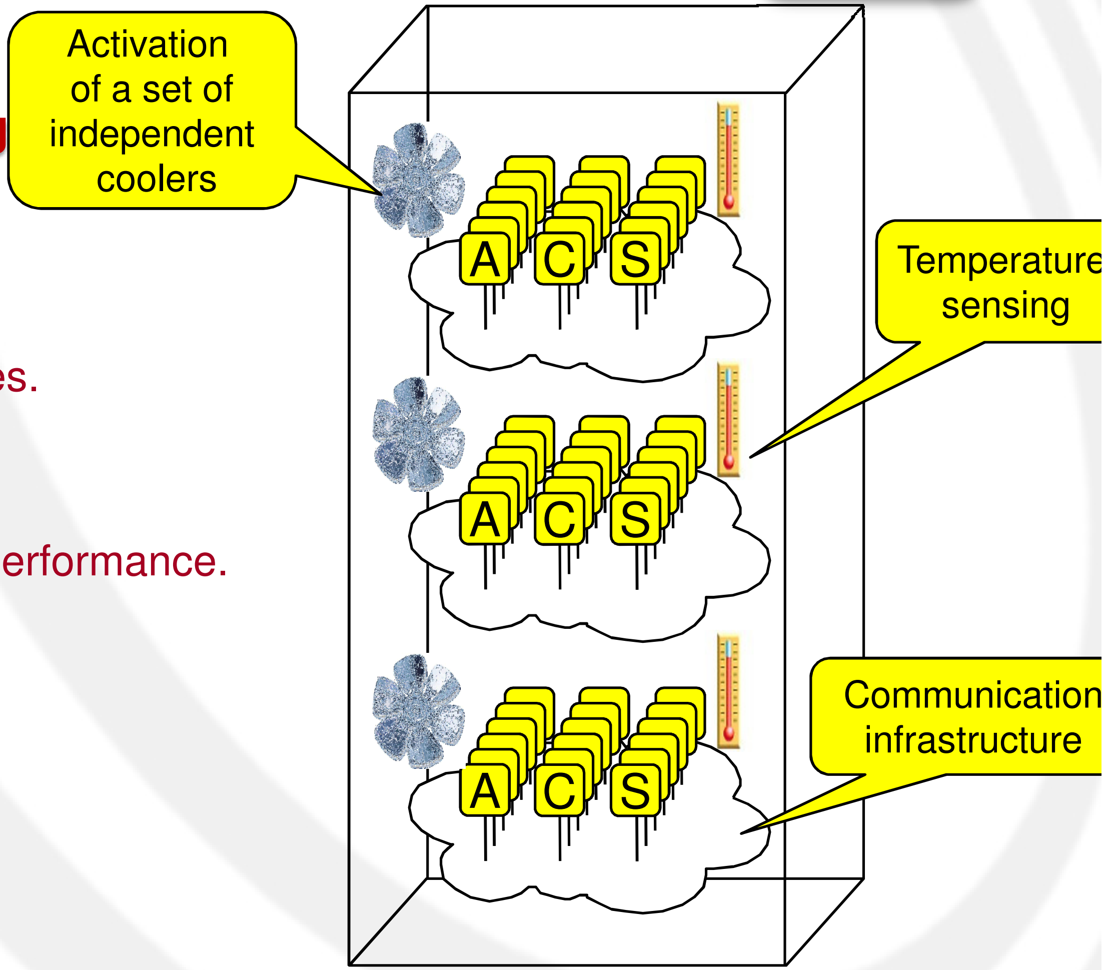
- **Networked Embedded Systems (NES)** are an important class of devices
  - Network functionalities are at the core of design objectives
  - Network requirements come together with traditional requirements
- **Distributed Embedded Systems** are group of NES which are connected together using network interfaces, standardized protocols and channels
  - Example: Temperature control of a building



Introduction

Temperature control of a building

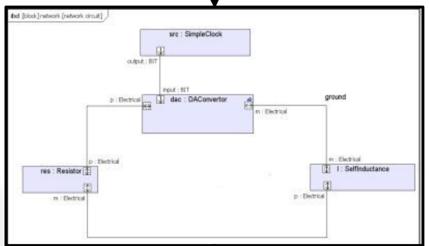
- Scenario:
  - Hundreds of concurrent tasks.
  - Heterogeneous tasks.
  - Devices with different capabilities.
  - Wireless and wired channels.
  - Many communication protocols.
  - Nodes position affects system performance.
- Questions:
  - How many nodes?
  - How to assign tasks to nodes?
  - Which network protocols?
  - Which intermediate systems?



Introduction

Traditional design flow for embedded systems:

Application requirements: functional & non-functional

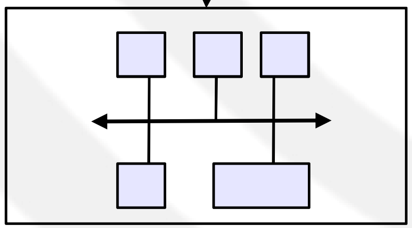


Model-driven design

Platform description:
IP blocks (CPU, memory, ASIC)

Design-space Exploration (DSE)

HW/SW partitioning

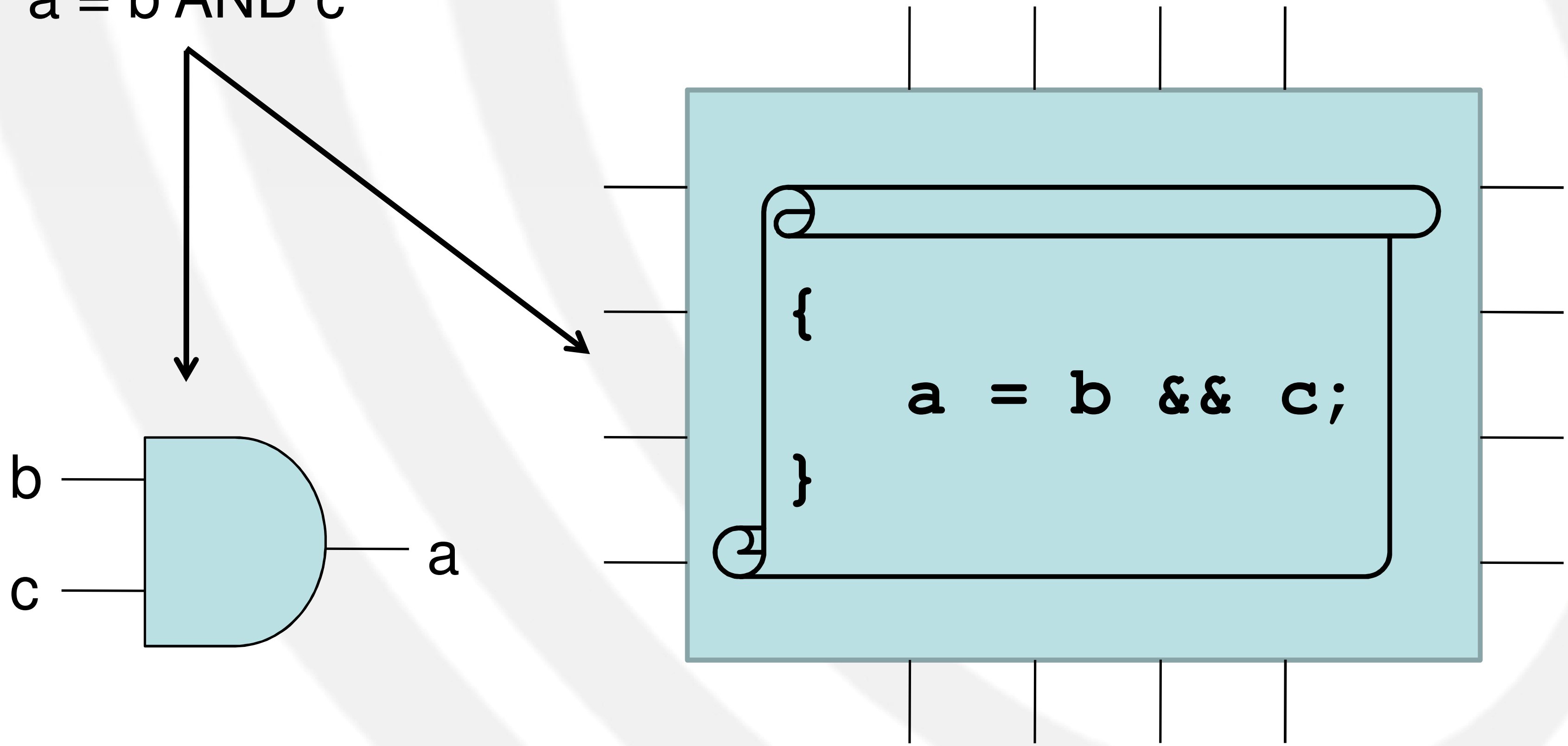


Final result

Introduction

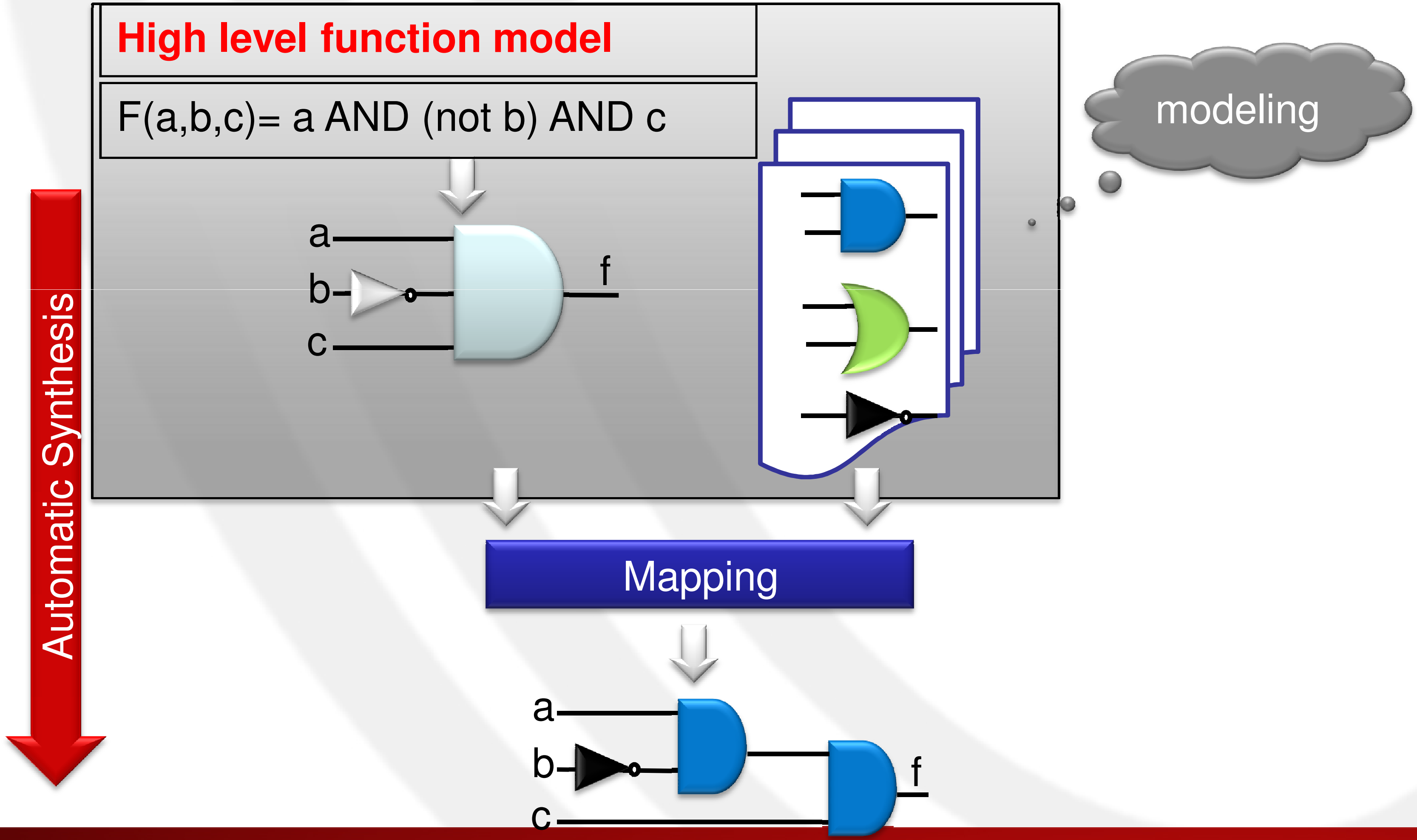
HW/SW partitioning:

a = b AND c



Introduction

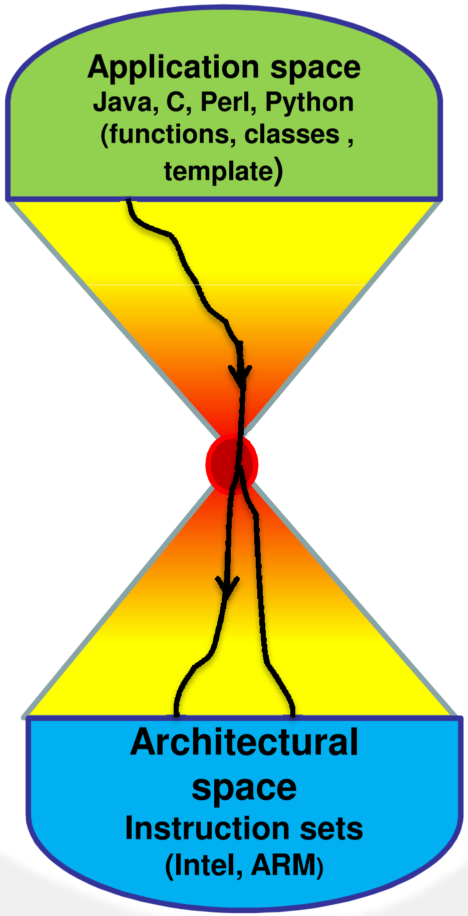
Hardware design:



Introduction

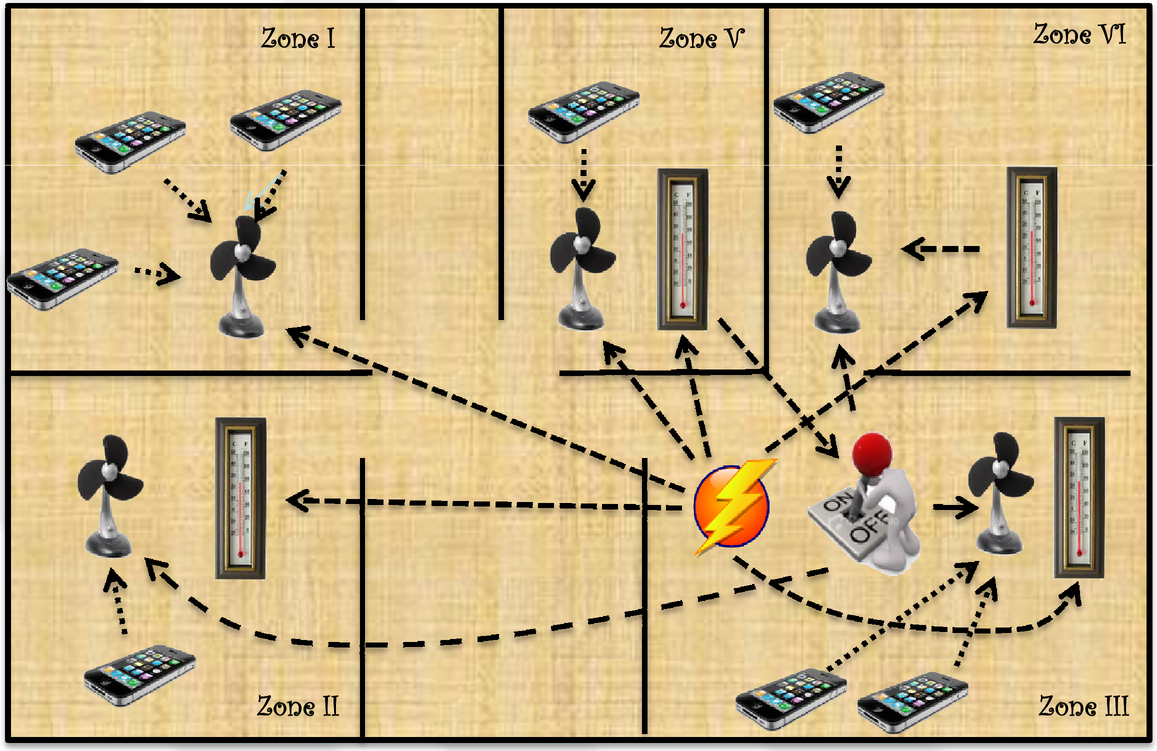
Software development

- Functionality is described with different languages and an automatic process is used to generate assembly code for different target CPU’s
- **Modeling** of the functionality: High level languages
- **Automatic synthesis**: Compilers



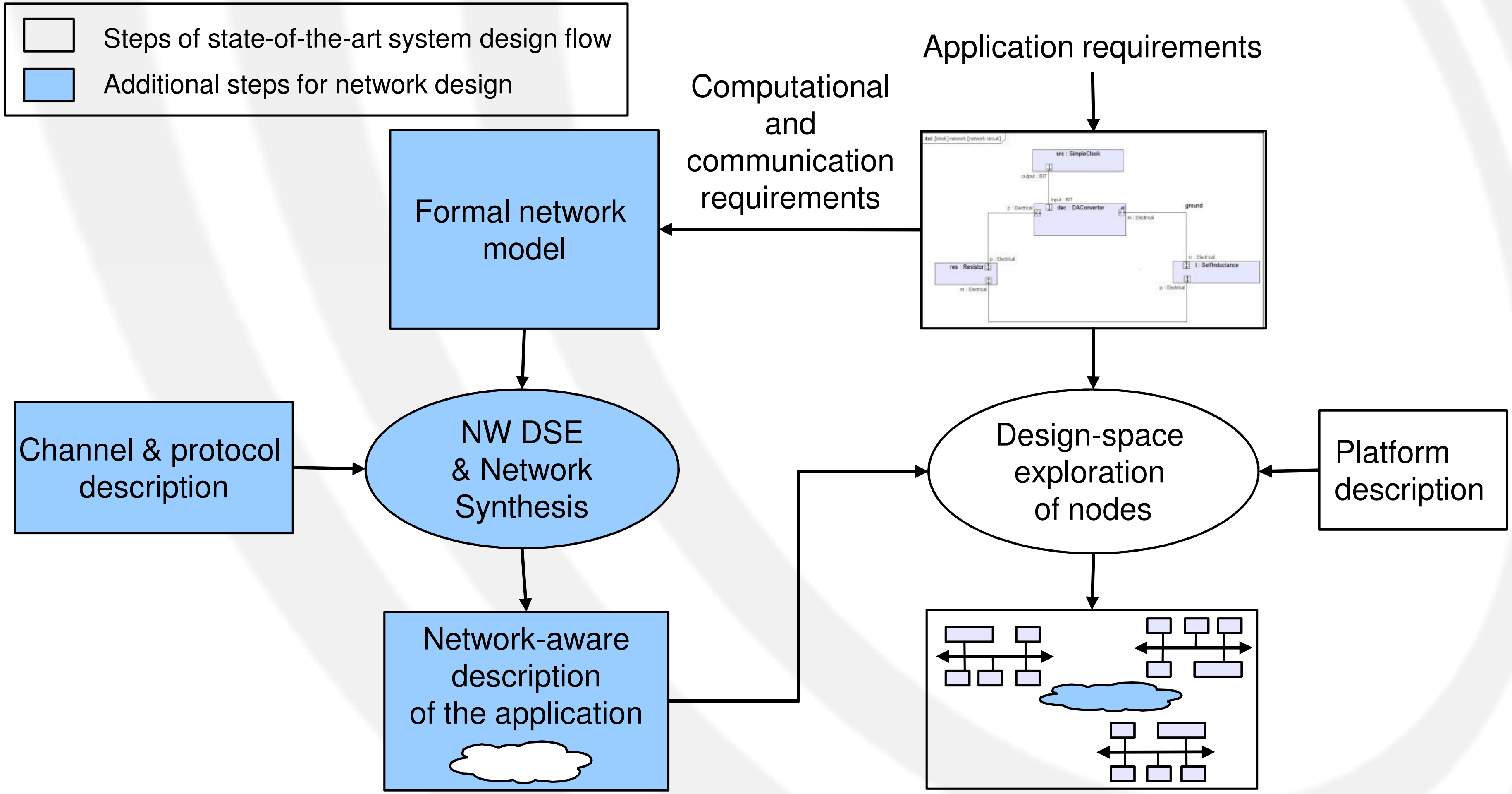
Introduction

- **Distributed embedded system** as a single system to be designed



Introduction

New design flow for NES



Introduction

- Start from an abstract Model-Based System Specification
- Modeling and Analysis of Real-Time and Embedded Systems (MARTE) profile for the unified modeling language (UML)
- Refinement steps and simulations
- Standard representation of requirement and solutions

UML MARTE

Background

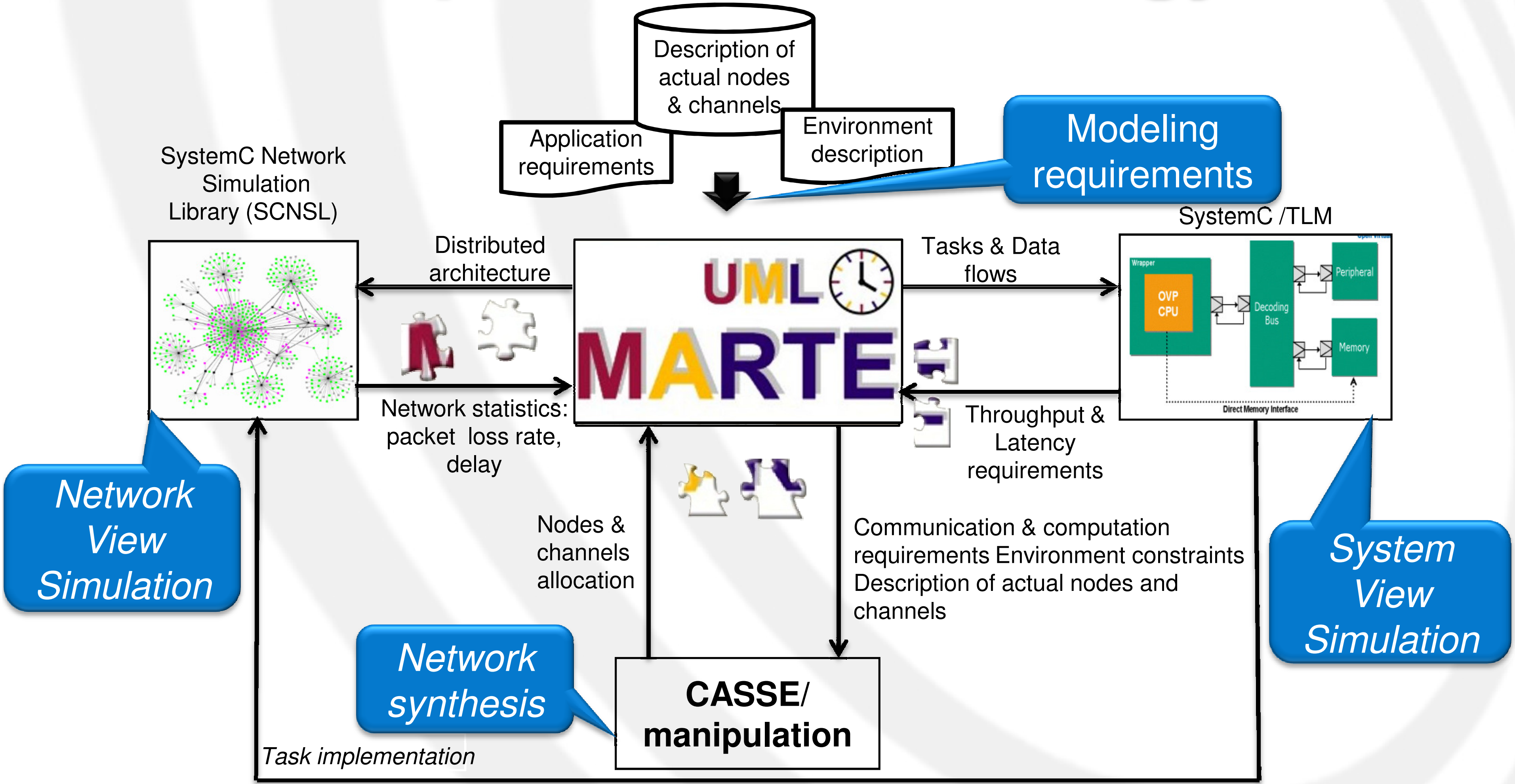
- Design of the network infrastructure starting from a library of nodes and channels (Network synthesis)
  - Communication Aware Specification and Synthesis Environment (CASSE), [FDL 2010]
  - COmmunication Synthesis Infrastructure framework (COSI), [IEEE TASE '12]
- **Open issue :** Both approaches do not rely on a standard representation of requirements (from the initial user specification) and solutions

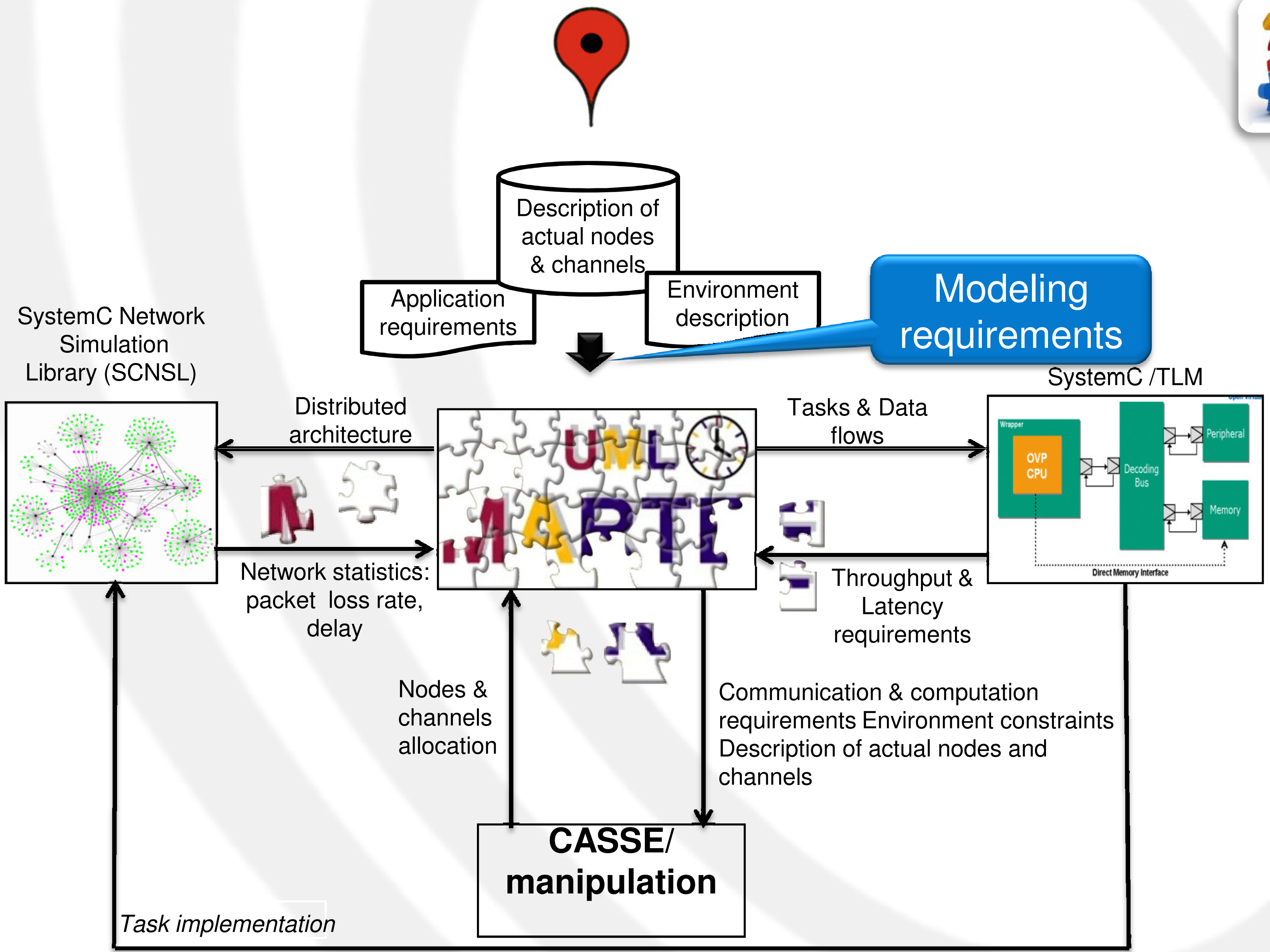
Key idea

Design methodology for networked embedded systems which combines UML/MARTE, network synthesis, and simulation

UML/MARTE not only at the starting point but also at the center of design flow as repository of refined version of the system up to the final solution

Proposed methodology




Description of actual nodes & channels
Application requirements
Environment description
Modeling requirements
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SystemC /TLM
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Tasks & Data flows
UML MARTE
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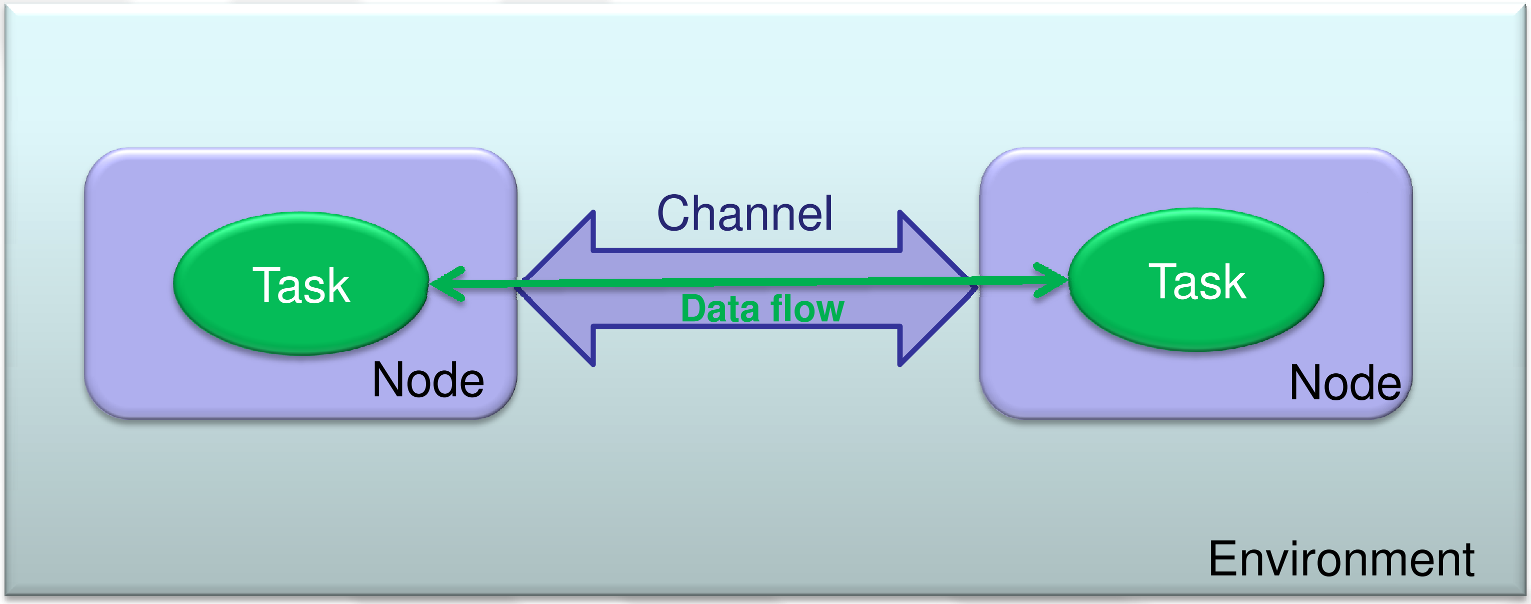
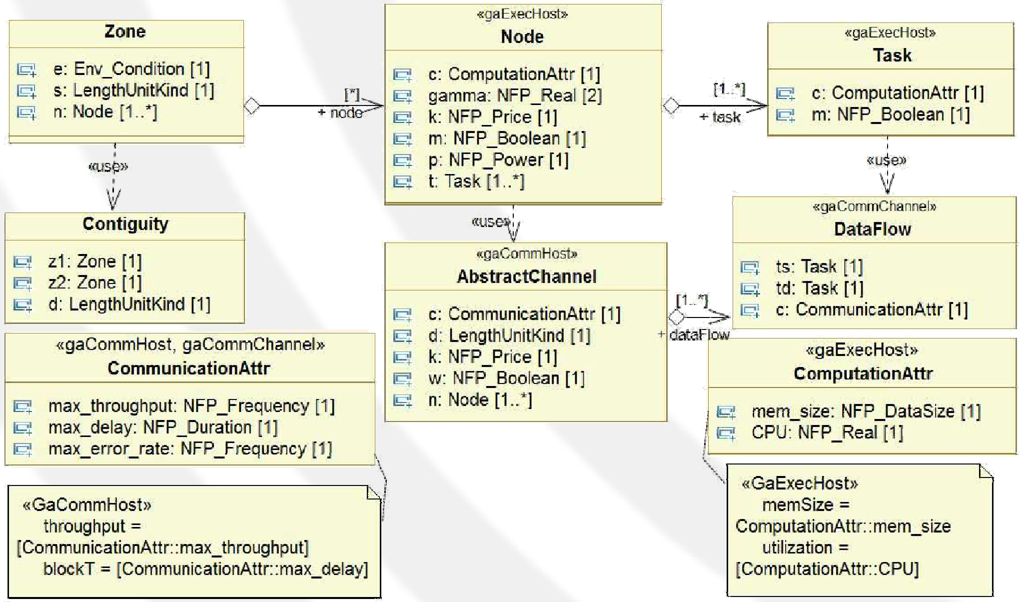
Modeling requirements

- The main aspects to be represented in UML/MARTE are:
  - Tasks, data flows, nodes, channels and the external environment



Modeling requirements

- Generic Quantitative Analysis Modeling (GQAM) sub-profile of MARTE profile are used to specify the semantics of some classes and their attributes
- This is the first time that GQAM is used to model the network



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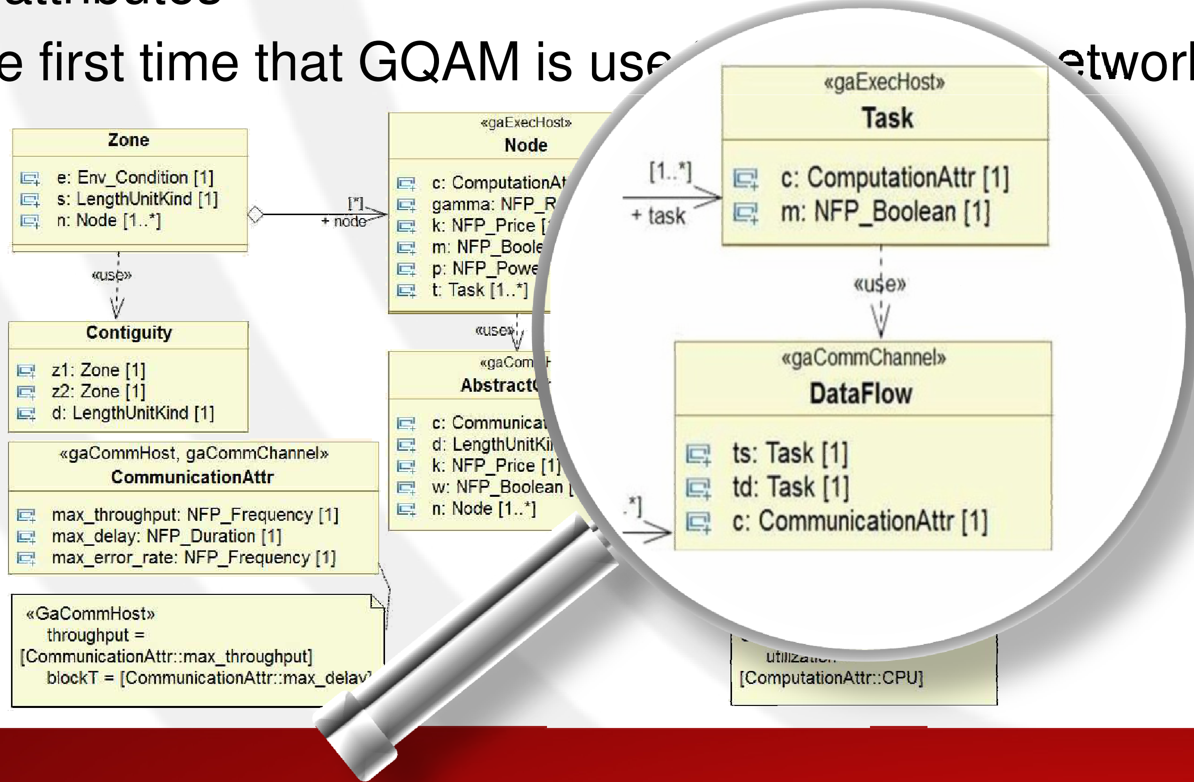

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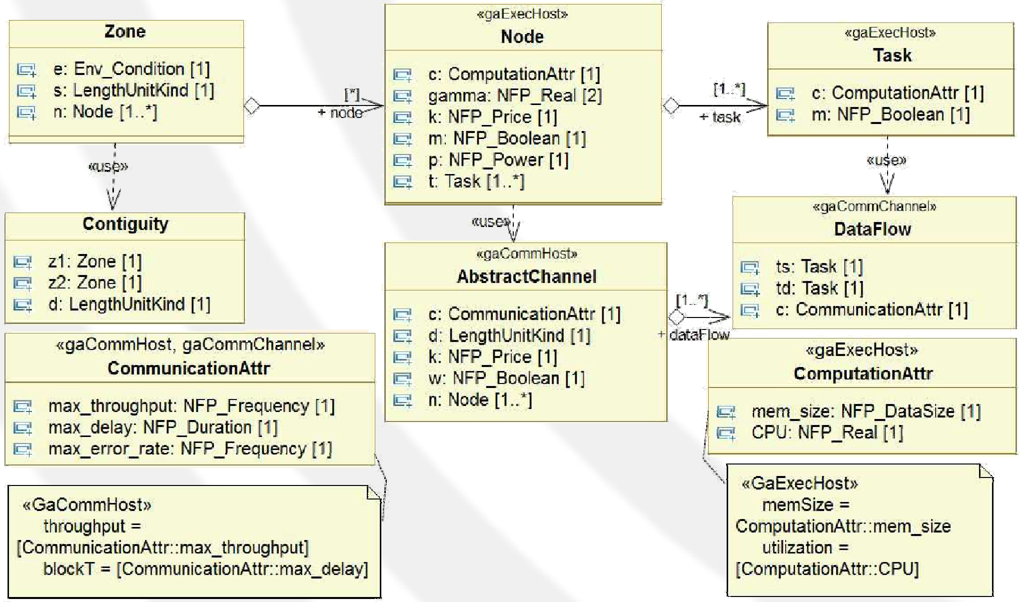

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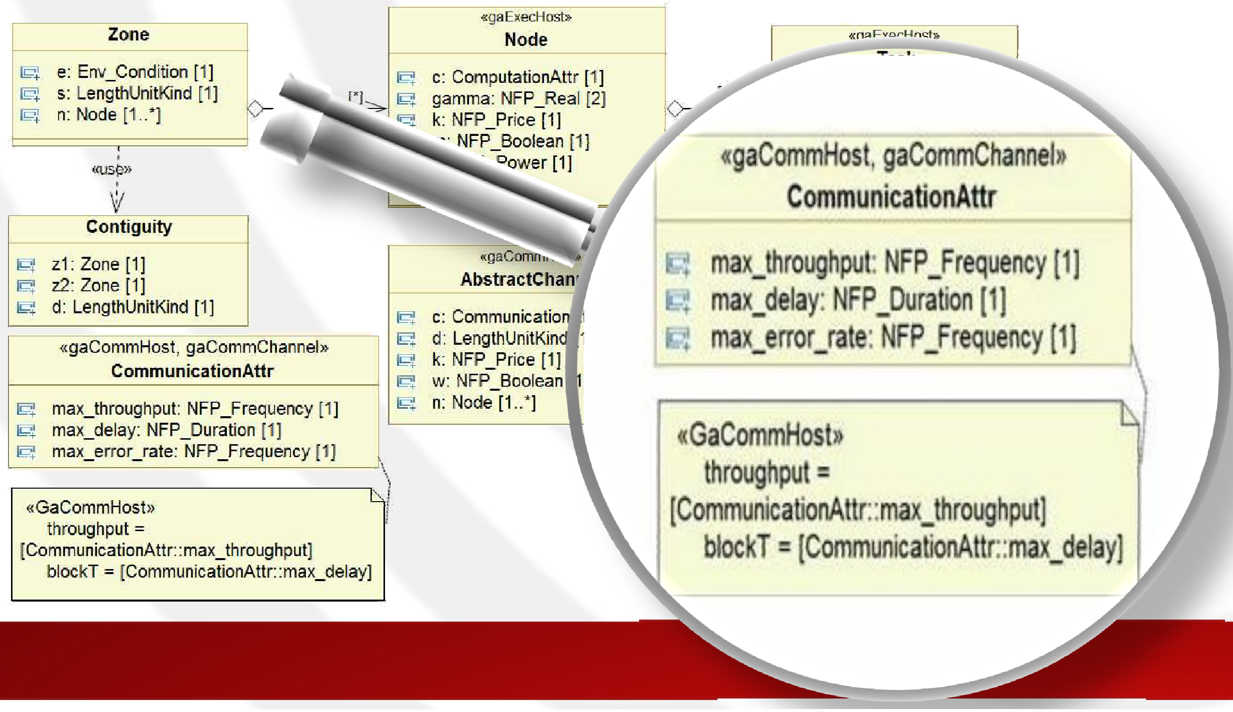

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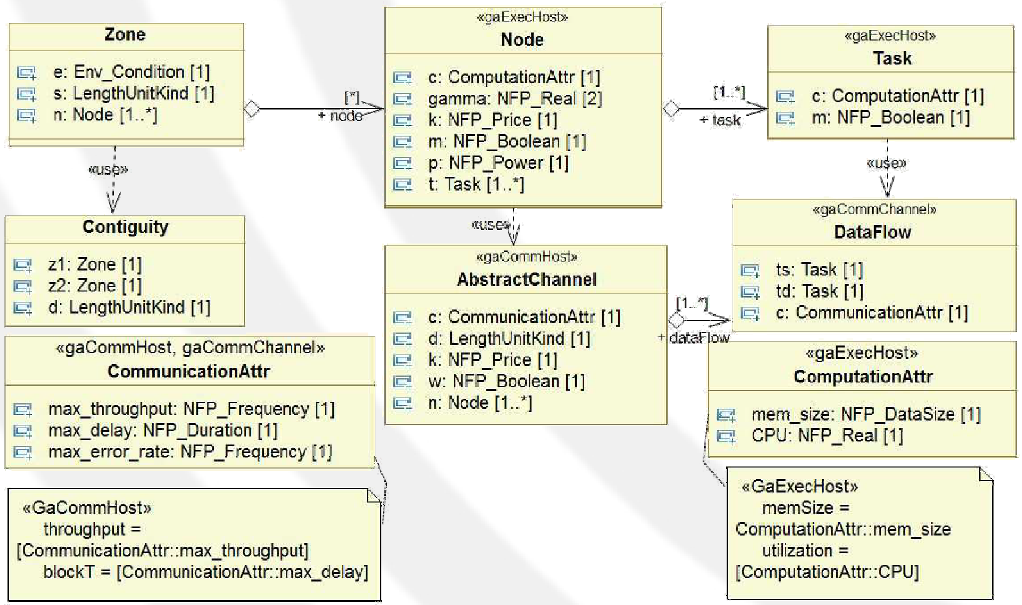

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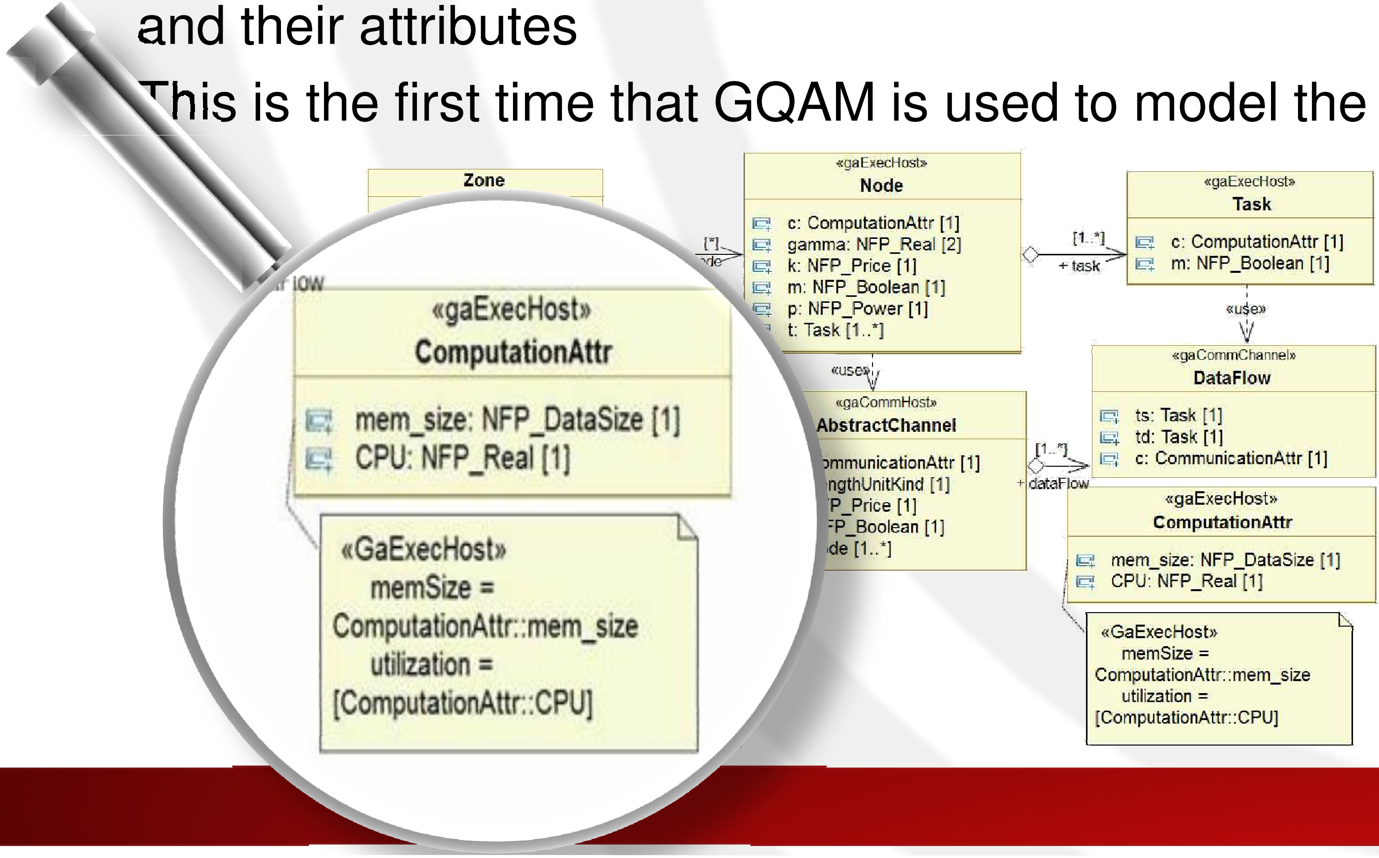
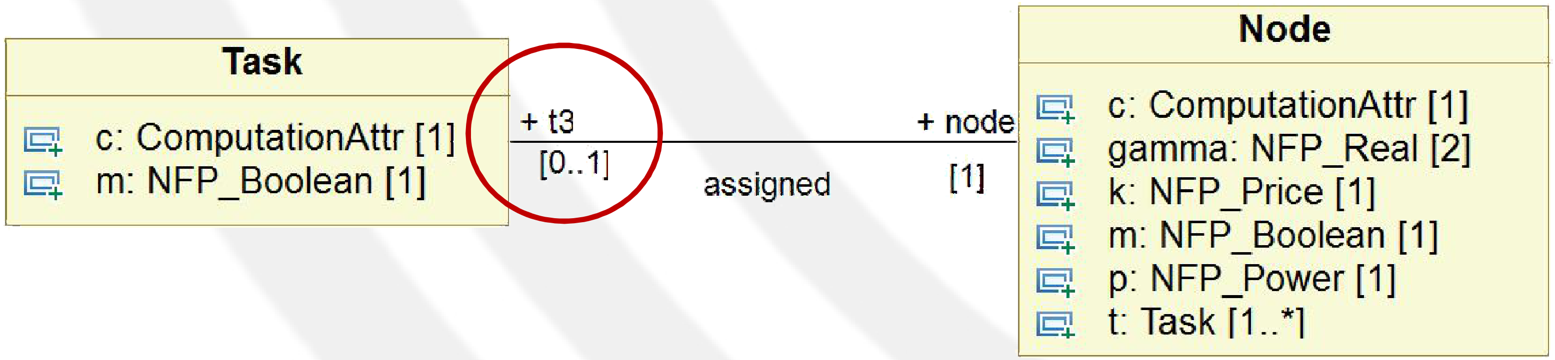
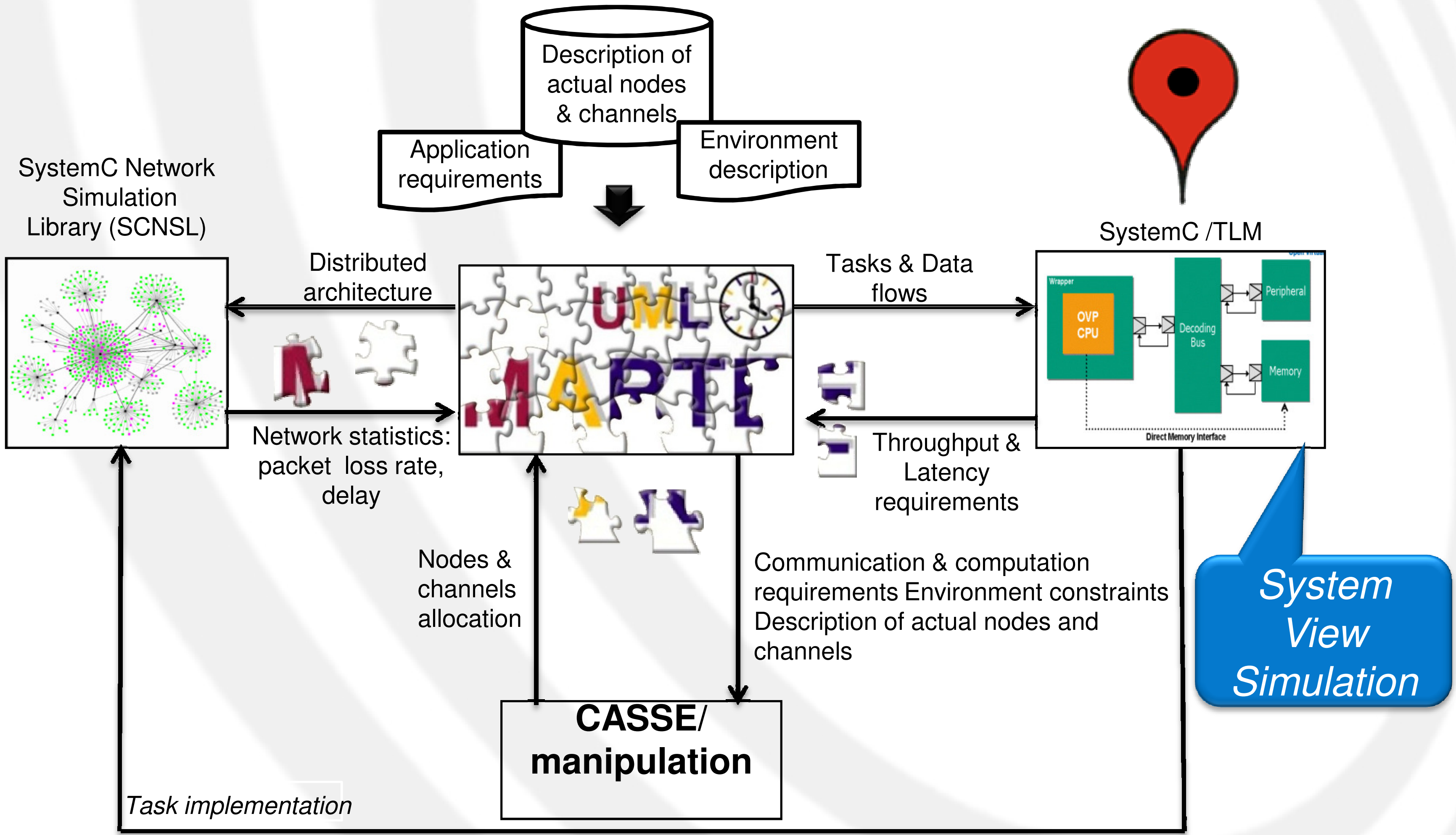


Modeling requirements

- Modeling of constraint:
  - Application constraints are specified by using cardinality on the relationships between classes
- Example of constraint: *"maximum one instance of t3 can be assigned to a single node"*

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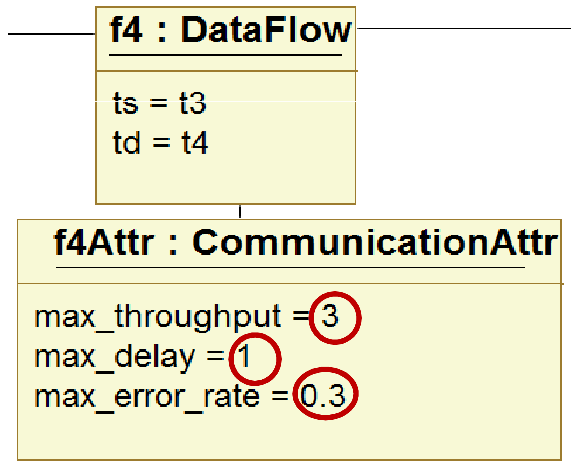
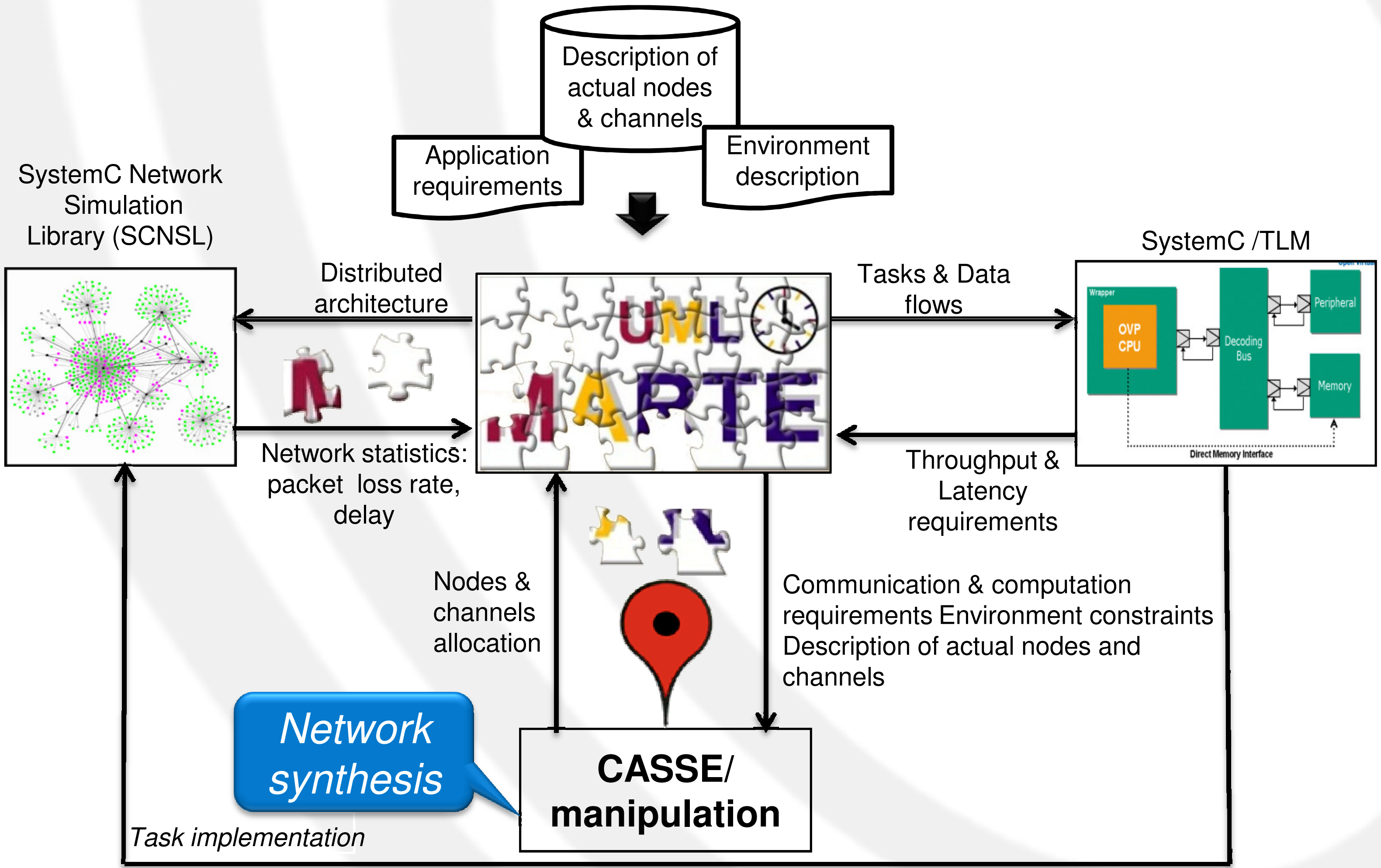
System view simulation

- UML/MARTE class diagram is extracted and used to generate SystemC/TLM model
  - Transformations are straight forward also (Villar,2009 and Vanderperren,2008)
- Execution of the SystemC model
  - Validate of functional behavior of the application
  - Fine-tune implementation details such as the content of exchanged messages and their sending rates
- Back annotation of throughput, latency and max error rate inside UML/MARTE model

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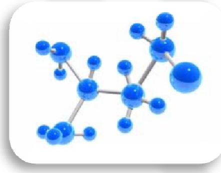
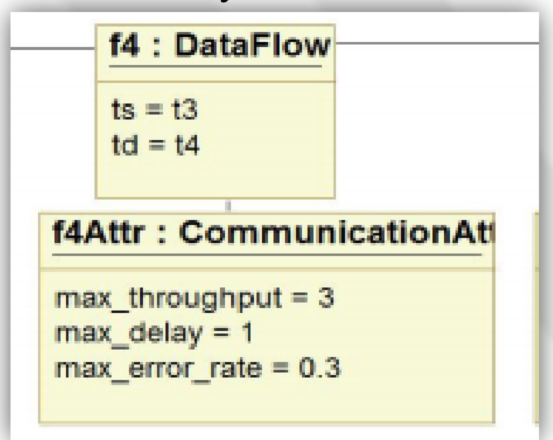
Network synthesis



- All the information about user constraints, communication requirements and actual channels and nodes are extracted from the UML/MARTE model and translated into Network synthesis mathematical representation
- CASSE provides a mathematical notation to specify the network dimension of a distributed embedded system, preparing the way for network synthesis



Dataflow(f4) = [t3, t4, [3, 1, 0.3]].

Network synthesis cont'd

Set of tasks & data flows

t3 : Task
c = 1,1
m = true

f4 : DataFlow
ts = t3
td = t4
c = 3,1,0.3

The building geometry

z3 : Zone

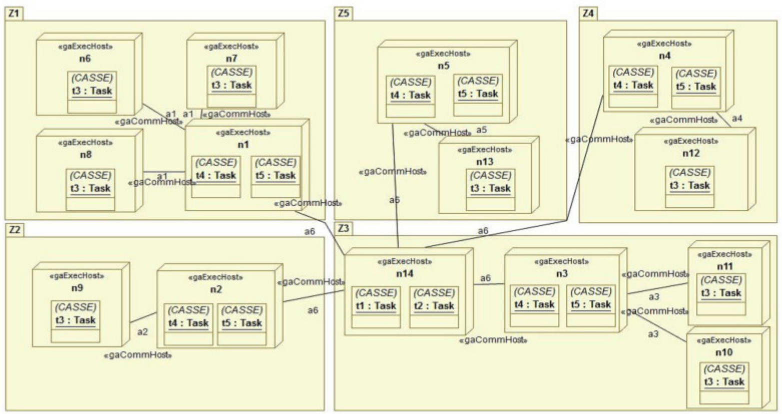
Technological library
(network nodes and channels)

b : Node
c = 10,10
gamma = [0.6, 0.9]
m = false
k = 100

y : AbstractChannel
c = 54,2,0.1
d = 30
w = true
k = 20

NW Synthesis

UML deployment diagram:
Assignment of *tasks inside nodes* and *data flows inside channels*



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NW Synthesis

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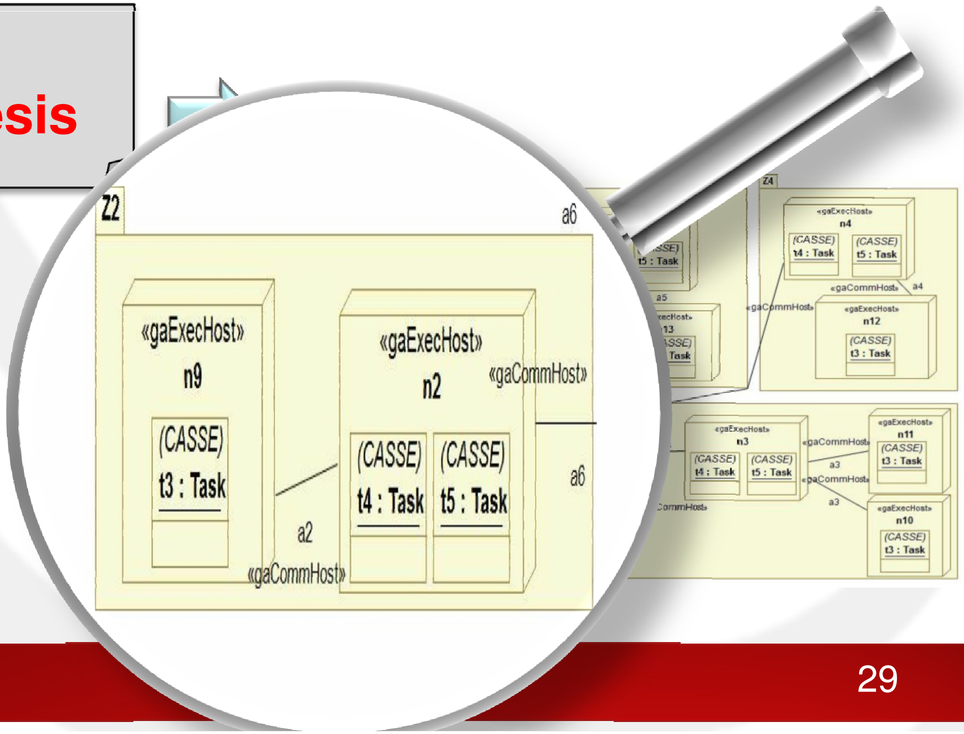
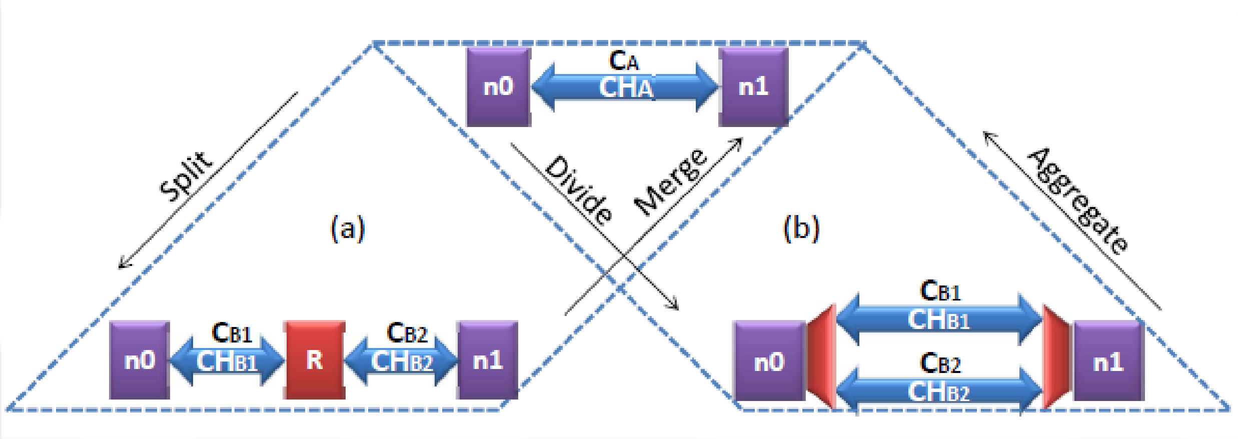
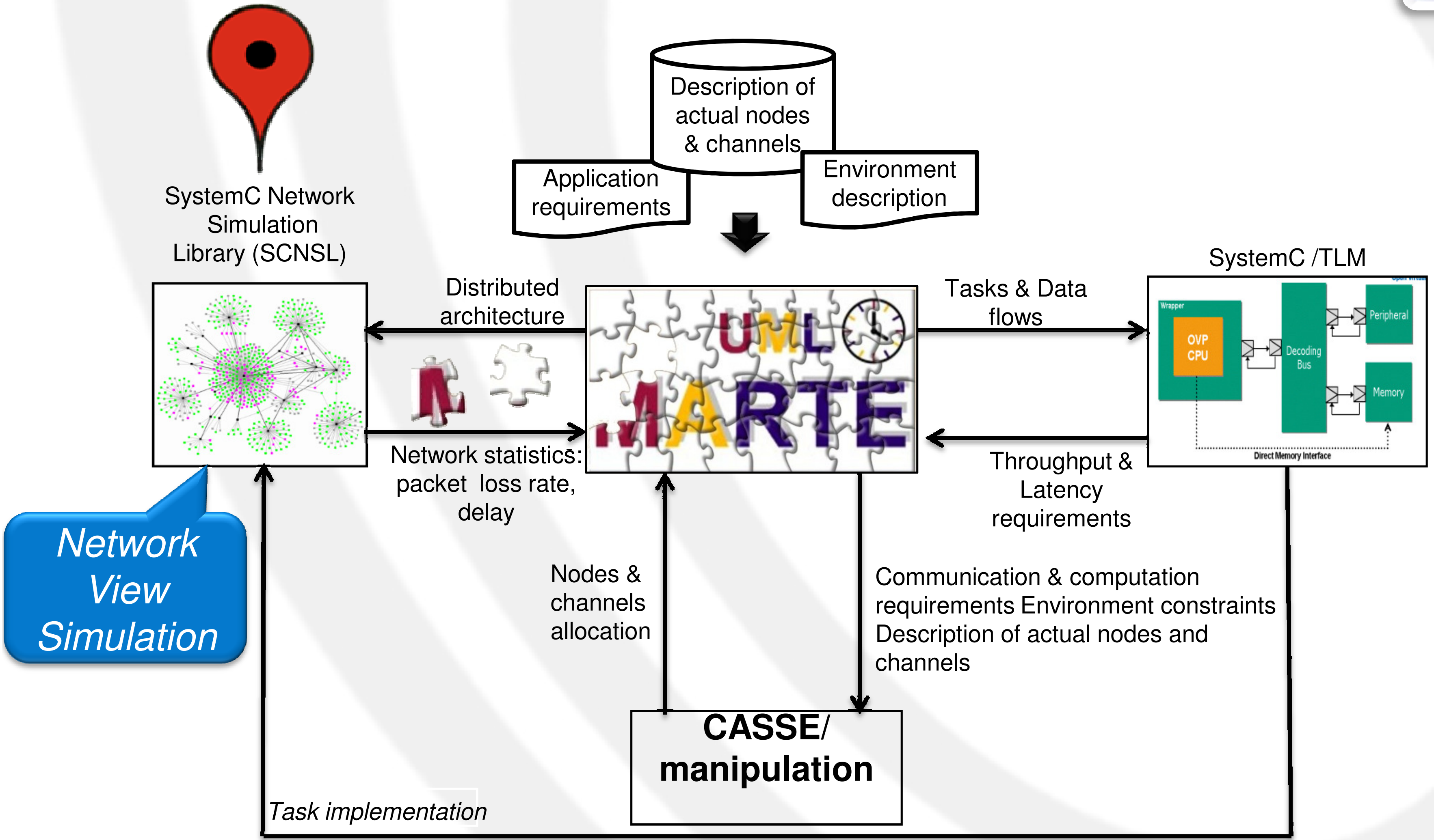


Manipulation

- This step aims at obtaining several NW alternatives which are equivalent from the network perspective
- Mathematical-based rules
  - Divide
  - Split
  - Merge
  - Aggregate





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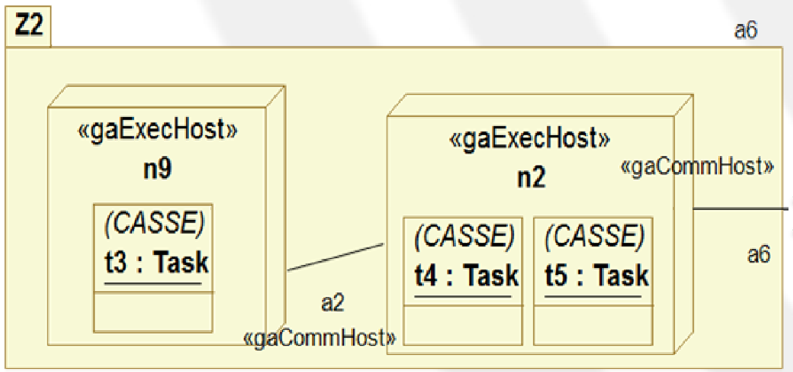
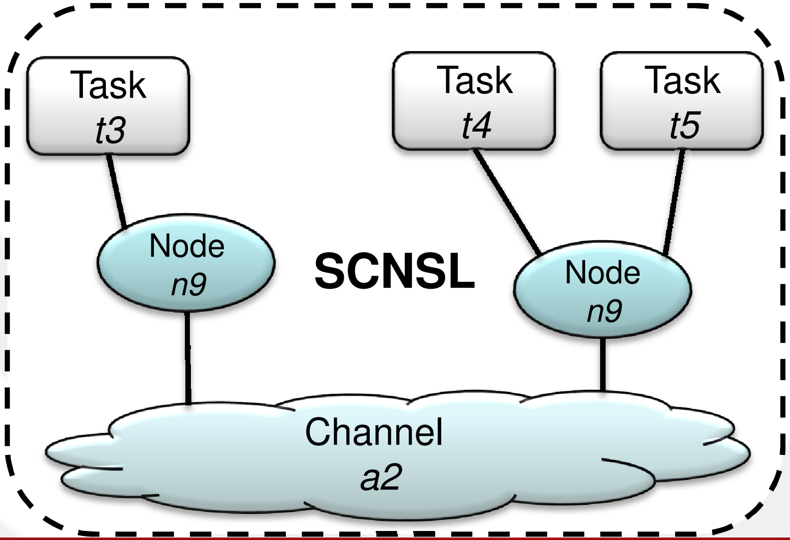
Network view simulation

- SCNSL is an extension of SystemC to allow modeling packet-based networks
  - It allows the easy and complete modeling of distributed applications of networked embedded systems such as wireless sensor networks, routers, and distributed plant controllers



UML deployment diagram



Network view simulation

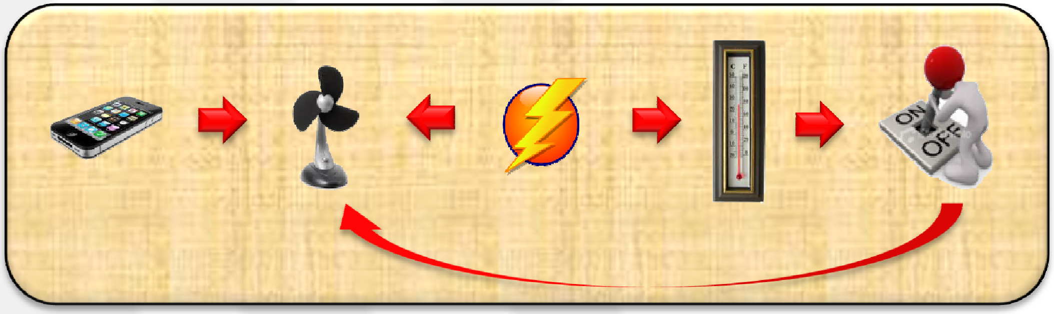
- Correspondence between UML/MARTE and SCNSL elements

UML/MARTE	SCNSL
Node (n1)	n1 = scnsl->createNode();

Channel (ch)
bound to node (n1)
	CoreChannelSetup t ccs;
	ch = scnsl->createChannel(ccs);
	BindSetup base t bsb1;
	scnsl->bind(n1,ch,bsb1);

Data flow between task (t1)
and task (t2)
	CoreCommunicatorSetup t ccoms;
	mac1 = scnsl ->createCommunicator(ccoms);
	scnsl->bind(& t1,& t2,ch,bsb1,mac1);

Case study



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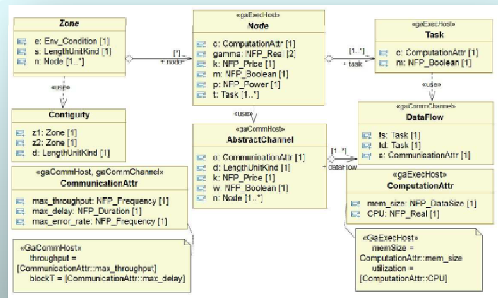
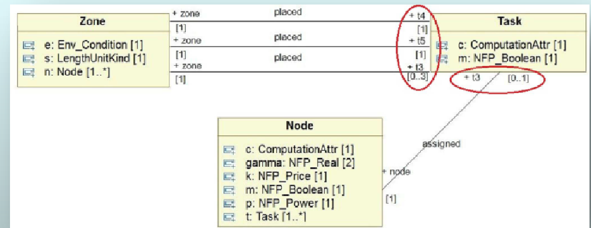
- one instance of actuator should be placed in each zone
- max……

User requirement



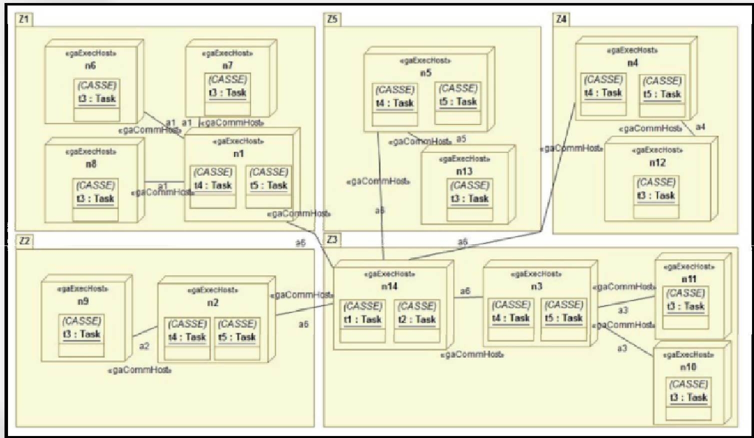


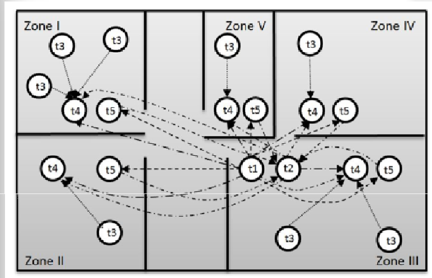
System View modeling

NW synthesis tool

Case study cont'd

NW view modeling

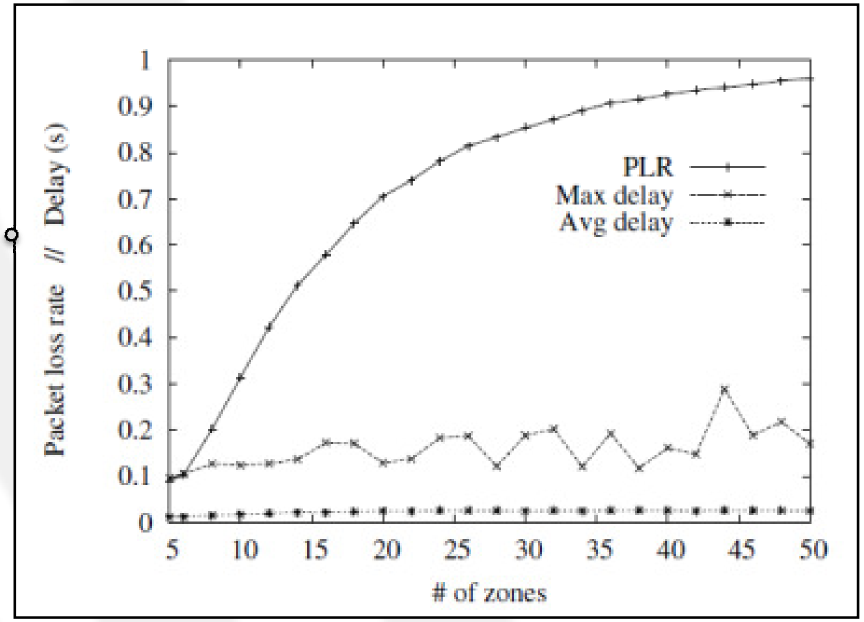




Network simulator (SCNSL)

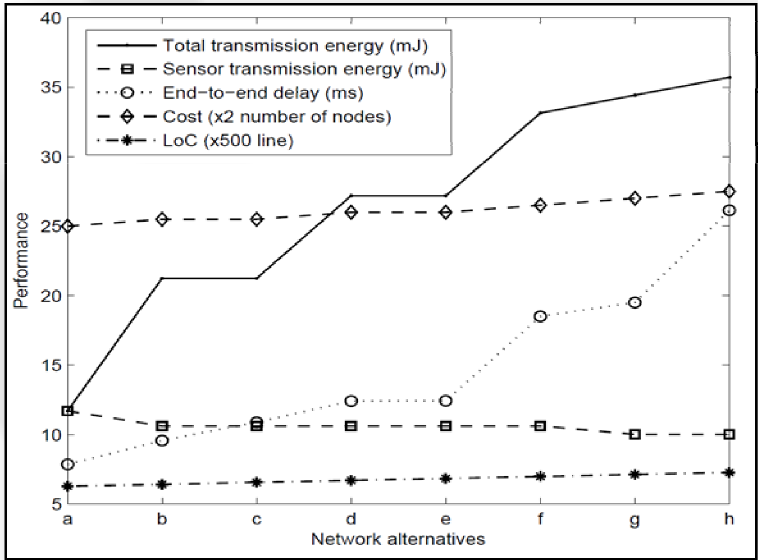
Case study cont'd

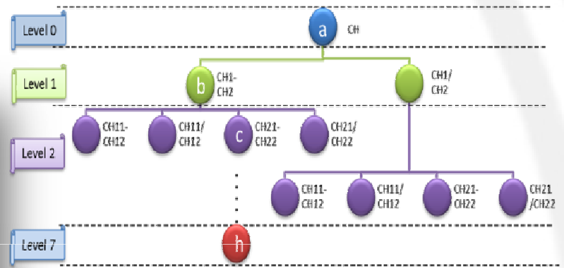
NW simulation statistics



Case study cont'd

NW simulation statistics





NW manipulation

Summary

- User requirements and constraints has been modeled by using UML/MARTE profile and simulated by SystemC/TLM at system view level
- Simulation results has been used to refine the user model
- Network synthesis tools have been used to solve the application problem
- Network solutions have been modeled and simulated by using SCNSL
- Network statistics have been used for the final refinement of application model
- **M**anipulation and **A**utomatic design-space exploration

Conclusions

- Some UML/MARTE diagrams and stereotypes have been used as a first time to represent the building blocks of a distributed embedded application
  - Elements from the MARTE specification have been applied to the context of distributed embedded applications
- Some gaps in MARTE standard have been identified concerning the representation of constraints and attributes related to error rate information
- SystemC code has been generated for both functional and network-aware simulation

A UML-centric design flow for networked embedded systems has been created